UPPSC Polytechnic Lecturer Syllabus

COMPUTER

Paper –I

1. **Computer Organization and Architecture :** Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register bus and memory transfer, Processor organization, general registers organization, stack organization and addressing modes. Arithmetic and Logic Unit, Control Unit, Memory, Input/output devices, interfaces and ports, Interrupts and exceptions. Modes of Data Transfer, Synchronous & asynchronous communication, standard communication interfaces.
2. **Data Structures :** Elementary Data Organization, Built in Data Types in C/C++/JAVA. Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations : Big Oh, Big Theta and Big Omega, Time-Space trade-off. Abstract Data Types (ADT), Arrays and Application of arrays, parse Matrices and their representations. Linked lists, Stacks, Queues, Searching and sorting Graphs, Tree, Binary Tree and its applications, Hashing, B+ tree.
3. **Discrete Structures & Theory of Logic :** Set Theory, Relations, Functions, Natural Numbers, Proof Methods, Proof counter – example, Proof by contradiction. Algebraic Structures, Lattices, Propositional Logic, Graphs, Combinatorics.
4. **Database Management Systems :** Database System vs File System, Database System Concept and Architecture, Data Model Schema and Instances, Data Independence and Database Language and Interfaces, Data Definitions Language, DML, Overall Database Structure. Data Modeling Using the Entity Relationship and enhanced E-R, Relational data Model and Language, Relational Algebra, Relational Calculus, Tuple and Domain Calculus. SQL, Data Base Design & Normalization, NoSQL, Transaction Processing, Concurrency Control Techniques, Web Interface to DBMS, OO database, Case Studies of commercial DBMS.
5. **Design and Analysis of Algorithm :** Algorithms and its analysis, Complexity of Algorithms, Growth of Functions, Performance Measurements, Sorting and Order Statistics, Red-Black Trees, B-Trees, Binomial Heaps, Fibonacci Heaps, Tries, Skip List, Divide and Conquer with Examples Such as Sorting, Matrix Multiplication, Convex Hull and Searching. Greedy Methods : Optimal Reliability Allocation, Knapsack, Minimum Spanning Trees – Prim's and Kruskal's Algorithms, Single Source Shortest Paths –Dijkstra's and Bellman Ford Algorithms, Dynamic Programming such as Knapsack. All Pair Shortest Paths – Warshal's and Floyd's Algorithms, Resource Allocation Problem. Backtracking, Branch and Bound techniques such as Travelling Salesman Problem, Graph Coloring, n-Queen Problem, Hamiltonian Cycles and Sum of Subsets. Algebraic Computation, Fast Fourier Transform, String Matching, Theory of NP-Completeness, Approximation Algorithms and Randomized Algorithms.
6. **Computer Networks :** Goals and Applications of Networks, Network structure and architecture, The OSI reference model, services, Network Topology Design, Physical Layer Transmission Media, Switching methods, ISDN, Terminal Handling, Medium Access sub layer – Channel Allocations, LAN protocols – ALOHA protocols – Overview of IEEE standards – FDDI. Data Link Layer – Elementary Data Link Protocols, Sliding Window protocols, Error Handling. Network Layer – Point – to Point Networks, routing, Congestion control Internetworking – TCP/IP, IP packet, IP address, IPv6. Transport Layer – Design issues,

connection management, Session Layer-Design issues, remote procedure call, Presentation Layer-Design issues, Data compression techniques, cryptography – TCP – Window Management. Application Layer : File Transfer, Access and Management, Electronic mail, Virtual Terminals, Other application. Internet and Public Networks, Peer to Peer Network.

7. **Principles of Programming Languages :** Role of Programming Languages, Programming Paradigms, Programming Environments, Language Description : Syntactic Structure, Language Translation Issues : Programming Language Syntax, Stages in Translation, Formal Translation Models, Data Types, and Basic Statements, Binding, Type Checking, Scope, Scope Rules, Lifetime and Garbage Collection, Primitive Data Types, Strings, Array Types, Associative Arrays, Record Types, Union Types, Pointers and References, Arithmetic Expressions, Overloaded Operators, Type Conversions, Relational and Boolean Expression, Assignment Statements, Mixed Mode Assignments, Control Structures, Selection, Iterations, Branching, Guarded Statements, Subprograms and Implementations, Design Issues for Functions, Semantics of Call and Return, Implementing Simple Subprograms, Stack and Dynamic Local Variables, Nested Subprograms, Dynamic Scoping. Object-Orientation, Concurrency and Event Handling, Object Oriented Programming using C++ and Java, Functional and Logic Programming Languages.

8. **Software Project Management :** Fundamentals of Software Project Management (SPM), Software Project Planning, Software Project Estimation, Project Organization and Scheduling Project Elements, Project Life Cycle and Product Life Cycle, Ways to Organize Personnel, Project Schedule, Scheduling Objectives, Building the Project Schedule, Scheduling Terminology and Techniques, Network Diagrams : PERT, CPM, Bar Charts : Earned Value Analysis, Earned Value Indicators : Budgeted Cost for Work Scheduled (BCWS), Cost Variance (CV), Schedule Variance (SV), Cost Performance Index (CPI), Schedule Performance Index (SPI), Interpretation of Earned Value Indicators, Error Tracking, Software Reviews, Software Quality Assurance and Testing, Project Management and Project Management Tools, Software Configuration Management, Risk Management, Cost Benefit Analysis, SPM Tools : CASE Tools, Planning and Scheduling Tools, MS-Project.

9. **Cyber Security :** Information Systems, its types and development, Information Security and its Need, Threats to Information Systems, Information Assurance, Cyber Security, and Security Risk Analysis Application Security : Database, E-mail and Internet, Data Security Considerations : Backups, Archival Storage and Disposal of Data: Milestone Charts, Gantt Charts, Dimensions of Project, Monitoring & Control, Security Technology, Firewall and VPNs Intrusion Detection, Access Control, Security Threats-Viruses, Worms, Trojan Horse, Bombs, Trapdoors, Spoofs, E-mail Viruses, Macro Viruses, Malicious Software, Network and Denial of Service Attack, Security Threats to E-Commerce-Electronic Payment System, e-Cash, Credit/Debit Cards. Digital Signature, Public Key Cryptography, Developing Secure Information Systems, Information Security Governance & Risk Management, Security Architecture & Design Security Issues in Hardware, Data Storage & Downloadable Devices, Physical Security of IT Assets, Access Control, CCTV and Intrusion Detection Systems, Backup Security Measures. Security Policies : Development of Policies, WWW Policies, Email Security Policies, Policy Review Process-Corporate Policies-Sample Security Policies, Publishing and Notification Requirement of the Policies. Evolving Technology Security – Mobile, Cloud, Outsourcing, SCM, Information Security Standards : ISO, IT Act, Copyright Act, Patent Law, IPR, Cyber Laws in India, IT Act 2000 Provisions, Intellectual Property Law, Software License, Semiconductor Law and Patent Law. Corporate Security.

10. **Theory of Computation :**

Paper–II

1. **Operating Systems :** Operating System definition, function and services, Types and features, Operating System Structure-Layered structure, System Components, Reentrant Kernels, Monolithic and Microkernel Systems, System Calls types, System Programs, Process and Thread : process states, process control block, Inter process communication; Process Synchronization : Classical problems of synchronization, Concurrent Processes CPU Scheduling Criteria and Algorithms, Memory Management, File management, Device Management and Disk scheduling, File Management, UNIX Commands and utilities, Linux : System components, Process management, scheduling, memory management, Networking software layers, Security, various editors, I/O devices, IPC.
2. **Computer Graphics :** Types of computer graphics, Graphic Displays, Random scan displays, Raster scan displays, Frame buffer and video controller, Points and lines drawing algorithms, Circle generating algorithms and parallel version of these algorithms, Basic and Composite Transformations, Reflections and shearing. Windowing and Clipping, 3-D Geometric Primitives, representation, Transformation, projections and Clipping, Curves and Surfaces, Hidden Lines and Surfaces.
3. **Artificial Intelligence :** Introduction, Foundations and History of Artificial Intelligence, Applications of Artificial Intelligence, Intelligent Agents, Structure of Intelligent Agents. Computer vision, Natural language Possessing, strategies, Informed search strategies and algorithms, Knowledge Representation & Reasoning Machine Learning, Pattern Recognition.
4. **Compiler Design :** Phases and passes, Bootstrapping, Finite state machines and regular expressions and their applications to lexical analysis, Optimization of DFA-Based Pattern Matchers implementation of lexical analysis, Formal grammars and their application to syntax analysis, BNF notation, ambiguity, YACC. The syntactic specification of programming languages : Context free grammars, derivation and parse trees, capabilities of CFG, Parsing Techniques, Syntax-directed Translation, Symbol Tables, Run-Time Administration, Error Detection & Recovery, Code Generation and Code optimization.
5. **Software Engineering :** Introduction, Software life-cycle models, Software requirements, Requirements Specification, Software design and Software user interface design, Coding Issues, Software integration and testing, Software support processes and Quality Assurance, IEEE Software Engineering Standards, Software maintenance, Software reuse, SOFTWARE TESTING & AUDIT.
6. **Distributed System :** Characterization of Distributed Systems, Theoretical Foundation for Distributed System, Distributed Mutual Exclusion, Distributed Deadlock Detection, Agreement Protocols, Distributed Resource Management, Failure Recovery in Distributed Systems, Transactions and Concurrency.
7. **Web Technologies :** Introduction and Web Development Strategies, Protocols Governing Web, Writing Web Projects, Internet services and tools, Client-server computing. Core Java, Web Page Designing, XML, DOM and SAX, Dynamic HTML, Scripting, Networking, Enterprise Java Bean, Java Database Connectivity (JDBC), Merging Data from Multiple Tables, Servlets, Handling HTTP get and post Requests, Redirecting Requests to Other Resources, Session Tracking, Cookies, Session Tracking with Http Session, Java Server Pages (JSP)
8. **Image Processing : Digital Image Fundamentals :** Steps in Digital Image Processing–Components–Elements of Visual Perception – Image Sensing and Acquisition – Image Sampling and Quantization – Relationships between pixels – Color image fundamentals – RGB, HSI models, Two-dimensional mathematical preliminaries, 2D transforms – DFT, DCT. **Image Enhancement :** Spatial Domain : Gray level transformations – Histogram processing – Basics of Spatial Filtering – Smoothing and Sharpening Spatial Filtering, Frequency Domain : Introduction to Fourier Transform – Smoothing and Sharpening frequency domain filters – Ideal, Butterworth and Gaussian filters, Homomorphic filtering, Color image enhancement. **Image Restoration :** Image Restoration – degradation model, Properties, Noise models – Mean Filters – Order Statistics – Adaptive filters – Band reject Filters – Band pass Filters – Notch Filters – Optimum Notch Filtering – Inverse Filtering – Wiener filtering, **Image Segmentation :** Edge detection, Edge linking via Hough transform – Thresholding – Region based segmentation – Region growing – Region splitting and merging – Morphological processing – erosion and dilation, Segmentation by morphological watersheds – basic concepts – Dam construction – Watershed segmentation algorithm. **Image Compression and Recognition :** Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, JPEG standard, MPEG. Boundary representation, Boundary description, Fourier Descriptor, Regional Descriptors – Topological feature, Texture – Patterns and Pattern classes – Recognition based on matching.
9. **Soft Computing :** Neural Networks, Fuzzy Logic and Genetic Algorithm (GA).
10. **High Performance Computing :** Grid Computing, Cluster Computing Beowulf Cluster, Cloud Computing.

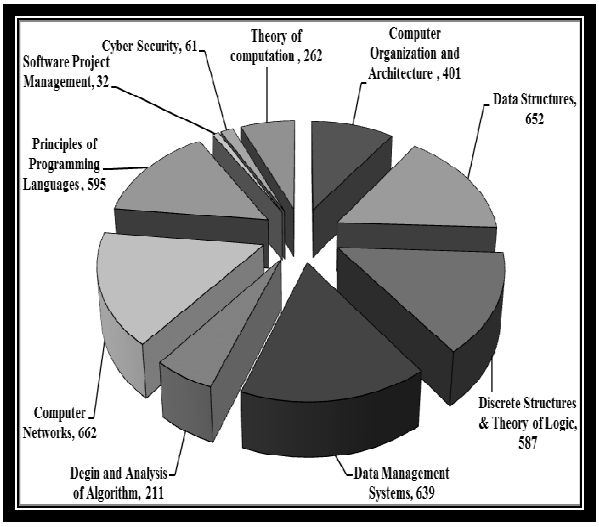
COMPUTER SCIENCE & ENGINEERING/INFORMATION TECHNOLOGY AE Previous Exam Papers Analysis Chart

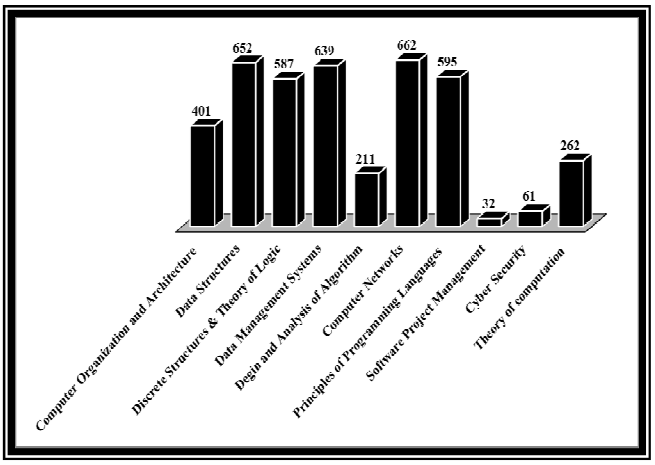
Sl No.	Exam	Proposed Year	Question Paper	Total Question
Uttar Pradesh Public Service Commission				
1.	UPPSC Asstt. Teacher (Trained Graduate Grade) LT Grade	29.07.2018		120
Uttar Pradesh Power Corporation Limited				
2.	UPPCL AE	2014		150
3.	UPPCL AE	18.05.2016		150
4.	UPPCL AE	12.11.2016		150
Union Public Service Commission				
5.	UPSC Senior Scientific Officer Grade - II	16.07.2017		100
6.	UPSC Poly. Lect.	10.03.2019		100
Graduate Aptitude Test in Engineering (GATE)				
7.	GATE	2021	Shift-I	55
8.	GATE	2021	Shift-II	55
9.	GATE	2020		55
10.	GATE	2019		55
11.	GATE	2018		55
12.	GATE	2017	Shift-I	55
13.	GATE	2017	Shift-II	55
14.	GATE	2016	Shift-I	55
15.	GATE	2016	Shift-II	55
16.	GATE	2015	Shift-I	55
17.	GATE	2015	Shift-II	55
18.	GATE	2015	Shift-III	55
19.	GATE	2014	Shift-I	55
20.	GATE	2014	Shift-II	55
21.	GATE	2014	Shift-III	55
22.	GATE	2013		55
23.	GATE	2012		55
24.	GATE	2011		55
Indian Space Research Organisation				
25.	ISRO Scientists/Engineer	12.01.2020		80
26.	ISRO Scientists/Engineer	22.04.2018		80
27.	ISRO Scientists/Engineer	27.05.2017		80
28.	ISRO Scientists/Engineer	17.12.2017		80
29.	ISRO Scientists/Engineer	03.07.2016		80
30.	ISRO Scientists/Engineer	11.10.2015		80
31.	ISRO Scientists/Engineer	24.05.2014		80
32.	ISRO Scientists/Engineer	12.05.2013		80
33.	ISRO Scientists/Engineer	2011		80
34.	ISRO Scientists/Engineer	2009		80
35.	ISRO Scientists/Engineer	2008		80
36.	ISRO Scientists/Engineer	2007		80
Rajasthan Public Service Commission				
37.	RPSC ACF & FRO Gr-I Comp. App./Science	23.02.2021		120
38.	RPSC ACF & FRO Gr-I Comp. Engg.	23.02.2021		120
39.	RPSC Vice Principal/Suptdt. (CS)	05.11.2019		100
40.	RPSC Vice Principal/Suptdt. (IT)	06.11.2019		100
41.	RPSC Vice Principal/Suptdt. (IT)	14.02.2016		100
42.	RPSC Vice Principal/Suptdt. (CS)	14.02.2016		100
43.	RPSC Lect.	2014		100
44.	RPSC Lect.	2011		100

Chhattisgarh PSC				
45.	CGPSC Asstt. Prof. (CS)	21.05.2016		100
46.	CGPSC Asstt. Prof. (Computer Application)	20.05.2016		100
47.	CGPSC Asstt. Prof. (IT)	31.05.2016		100
Gujarat Public Service Commission				
48.	GPSC Asstt. Prof.	30.06.2021		200
49.	GPSC Asstt. Manager (IT) (GMDC)	13.12.2020		200
50.	GPSC Asstt. Prof. (CS)	2016		100
51.	GPSC Asstt. Prof. (IT)	2016		100
Madhya Pradesh Public Service Commission				
52.	MPPSC Forest Service Exam	2014		150
National Institute of Electronics & Information Technology				
53.	NIELIT Scientists – B (CS)	22.07.2017		60
54.	NIELIT Scientists – B (IT)	22.07.2017		60
55.	NIELIT Scientists – B (CS)	04.12.2016		60
56.	NIELIT Scientists – B (IT)	04.12.2016		60
Bihar Public Service Commission				
57.	BPSC Asstt. Prof.	21.09.2021		80
Andhra Pradesh PSC				
58.	APPSC Lect. Comp. App. and Comp. Science (Degree College)	16.09.2021		150
59.	APPSC Poly. Lect.	13.03.2020		150
60.	APPSC Lect. Comp. Science (Degree College)	2016		150
61.	APPSC Lect. Comp. App. and Comp. Science (Degree College)	2016		150
Punjab Public Service Commission				
62.	PPSC Poly. Lect. (CS)	07.05.2017		100
63.	PPSC Poly. Lect. (IT)	2016		100
64.	PPSC Civil Supplies Corp. Ltd.	13.11.2011		100
65.	PPSC Network Engineer	2014		100
Kerala PSC				
66.	Kerala PSC Asstt. Prof.	27.10.2016		80
67.	Kerala PSC Asstt. Prof.	27.09.2016		80
68.	Kerala PSC Poly. Lect.	28.01.2015		80
69.	Kerala PSC Poly. Lect.	23.11.2015		80
Karnataka PSC				
70.	Karnataka PSC Computer Science Teacher	16.10.2017		100
71.	Karnataka Post Graduate Teacher	31.05.2017		100
72.	GESCOM AE	2011		100
Tamilnadu PSC				
73.	TNPSC Asstt. System Engineer & Asstt. System Analyst	2019		100
74.	TANGEDCO AE	2018		64
75.	TRB Poly. Lect. (CS)	2017		150
76.	TRB Poly. Lect. (IT)	2017		150
77.	TNPSC Deputy Manager (IT) Paper-I	2016		100
78.	TNPSC Deputy Manager (IT) Paper-II	2016		100
79.	TRB Asstt. Prof. (CS)	2014		150
Telangana PSC				
80.	TSPSC Manager	2015		150
			Total	**7514**

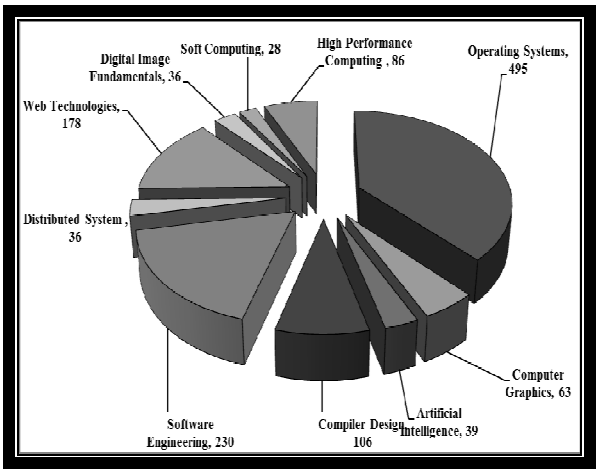
Trends Analysis of Computer Science Engineering and IT Through Pie Chart and Bar Graph

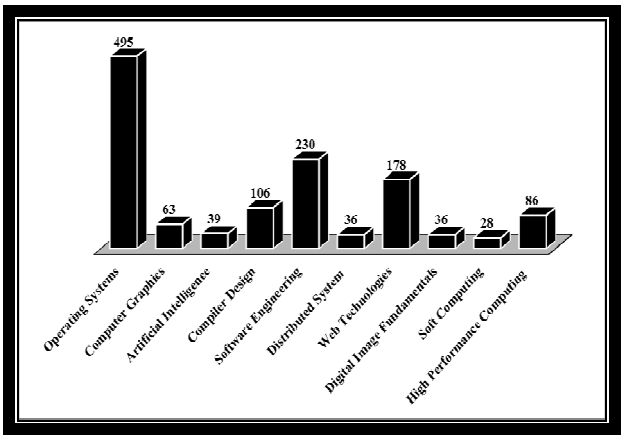
Paper-I





Paper-II





01. COMPUTER ORGANIZATION AND ARCHITECTURE

Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register bus and memory transfer, Processor organization, general registers organization, stack organization and addressing modes. Arithmetic and Logic Unit, Control Unit, Memory, Input/output devices, interfaces and ports, Interrupts and exceptions. Modes of Data Transfer, Synchronous & Asynchronous Communication, Standard Communication Interfaces.

1. Which is not a valid register of a DMA controller?

(a) Program counter (b) Word count register
(c) Control register (d) Address register

RPSC VPITI 2018 (CS)

Ans. (a) :

2. Which is not a valid characteristic of RISC processor ?

(a) Memory access limited to load/store instructions
(b) Variable length instruction formats
(c) Single cycle instruction execution
(d) Hardwired rather than microprogrammed control unit

RPSC VPITI 2018 (CS)

Ans. (b) :

3. A particular disk unit uses a bit string to record the occupancy or vacancy of its tracks, with 0 denoting vacant and 1 for occupied. A 32-bit segment of this string has hexadecimal value D4FE2003. The percentage of occupied tracks for the corresponding part of the disk, to the nearest percentage is

(a) 12 (b) 25
(c) 38 (d) 44

ISRO Scientist/Engineer 22.04.2018

Ans. (d) :

4. Disk requests come to a disk driver for cylinders in the order 10, 22, 20, 2, 40, 6 and 38, at a time when the disk drive is reading from cylinder 20. The seek time is 6 ms/cylinder. The total seek time, if the disk arm scheduling algorithms is first-come-first-served is

(a) 360 ms (b) 850 ms
(c) 900 ms (d) None of the above

ISRO Scientist/Engineer 22.04.2018

Ans. (d) :

5. What is the maximum number of characters (7 bits + parity) that can be transmitted in a second on a 19.2 kbps line. This asynchronous transmission require 1 start bit and 1 stop bit.

(a) 192 (b) 240
(c) 1920 (d) 1966

ISRO Scientist/Engineer 2013

Ans. (c) :

6. Two eight bit bytes 1100 0011 and 0100 1100 are added. What are the values of the overflow, carry and zero flags respectively, if the arithmetic unit of the CPU uses 2's complement form?

(a) 0, 1, 1' (b) 1, 1, 0
(c) 1, 0, 1 (d) 0, 1, 0

ISRO Scientist/Engineer 2013

Ans. (d) :

7. A processor is fetching instructions at the rate of 1 MIPS, A DMA module is used to transfer characters to RAM from a device transmitting at 9600 bps. How much time will the processor be slowed down due to DMA activity?

(a) 9.6 ms (b) 4.8 ms
(c) 2.4 ms (d) 1.2 ms

ISRO Scientist/Engineer 2013

Ans. (d) :

8. A pipeline P operating at 400 MHz has a speedup factor of 6 and operating at 70% efficiency. How many stages are there in the pipeline?

(a) 5 (b) 6 (c) 8 (d) 9

ISRO Scientist/Engineer 2013

Ans. (d) :

9. The number of address and data lines for a memory of 4K× 16 is:

(a) 12 and 16 (b) 10 and 16
(c) 12 and 12 (d) 16 and 16

TSPSC Manager 2015

Ans. (a) :

10. The most common technique used to reduce the disk accesses in a file system is known as:

(a) Buffer cache
(b) Long-structured file system
(c) LFS-cleaner
(d) Write-through caches

UPSC Poly Lect. 10.03.2019

Ans. (a) :

11. A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60-MHz clock. To service a cache miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block,

and finally transmits the words of the requested block at the rate of 1 word per cycle. The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is _____ × 10^6 bytes/sec.

GATE-2019

Ans. 160

12. Considering available memory blocks of size 20 KB and 15 KB, and allocation requests of 10 KB followed by 20 KB; which of the following memory allocation techniques will satisfy both requests?

I. Best fit
II. First fit
III. Worse fit

(a) Only I (b) Only II
(c) Only III (d) Both I and II
(e) Both I and III

CGPSC Asstt. Prof. 2014 (IT)

Ans. (a) :

13. Considering available memory blocks of size 20 KB and 15 KB, and allocation requests of 8 KB, 12 KB, and then 13 KB; which of the following memory allocation techniques will fail to satisfy all requests?

I. Best fit
II. First fit
III. Worse fit

(a) I, II and III (b) Both I and II
(c) Both I and III (d) Only II
(e) Both II and III

CGPSC Asstt. Prof. 2014 (IT)

Ans. (c) :

14. In MS-DOS, with respect to commands "MD" and "MKDIR", which of the following is true?

(a) "MD" will move directory and "MKDIR" will make directory
(b) "MD" will make directory and "MKDIR" will move directory
(c) "MD" will move file to directory and "MKDIR" will make directory
(d) Both have same functionality
(e) These are not MS-DOS commands

CGPSC Asstt. Prof. 2014 (IT)

Ans. (d) :

15. There are 200 tracks on a disk platter and the pending requests have come in the order–36, 69, 167, 76, 42, 51, 126, 12, and 199. Assume the arm is located at the 100th track and moving towards track 200. If sequence of disc access is 126, 167, 199, 12, 36, 42, 51, 69, and 76 then which disc access scheduling policy is used?

(a) Elevator
(b) shortest Seek-time First
(c) C-SCAN
(d) First Come First Served

ISRO Scientist/Engineer 2014

Ans. (c)

16. Disk requests are received by a disk drive for cylinder 5,25,18,3,39,8 and 35 in that order. A seek takes 5 msec per cylinder moved. How much seek time is needed to serve these requests for a Shortest Seek First (SSF) algorithm? Assume that the arm is at cylinder?,0 When the last of these requests is made with none of the requests yet served

(a) 125 msec (b) 295 msec
(c) 575 msec (d) 750 msec

ISRO Scientist/Engineer 2007

Ans. (b)

17. Back-up procedure helps in

(a) Restoring the operation whenever there is a disk failure
(b) Restoring both application and system software whenever there is disk corruption.
(c) Restoring the data files whenever there is a system crash
(d) All of the above

Punjab State Civil Supplies Corp. Ltd. 13.11.2011

Ans. (d) :

18. An application loads 100 libraries at start-up. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected):

(a) 0.50 s (b) 1.50 s
(c) 1.25 s (d) 1.00 s

Punjab PSC Lect. 2016 (IT)

Ans. (b) :

19. A CPU generally handles an interrupt by executing an interrupt service routine:

(a) As soon as an interrupt is raised
(b) By checking the interrupt register at the end of fetch cycle
(c) By checking the interrupt register after finishing the execution of the current instruction
(d) By checking the interrupt register at fixed time intervals

Punjab PSC Lect. 2016 (IT)

Ans. (c) :

20. How many bits are required in the operation code. If a Computer uses a memory unit with 1M words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts; an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

(a) 7 (b) 6
(c) 20 (d) 5

UPPCL AE 2014

Ans. (d) :

21. **A program on a particular computer takes 50ns to execute. The computer spends 80 percent of its time in execution. The manufacturer makes a change by a factor 8 to enhance the performance. What is the execution time after the change?**

(a) 41.25s (b) 15s
(c) 30s (d) 82.5s

UPPCL AE 2014

Ans. (b) :

22. **Which among the following is correct for the causes of pipeline conflict in pipelined processor?**

(i) Resource (ii) Data dependency (3) Branch difficulties (iv) control dependency

(a) i and iii (b) i, ii, iii, iv
(c) i and ii (d) i, ii, iii

UPPCL AE 2014

Ans. (c) :

23. **In a six stage pipeline assuming that there is no branch instructions. If we want to execute 15 instructions. What is time required to execute these instructions.**

(a) 16 (b) 15
(c) 21 (d) 20

UPPCL AE 2014

Ans. (d) :

24. **A computer handles several interrupt sources of which the following are relevant for this question.**

- **Interrupt from CPU temperature sensor (raises interrupt if CPU temperature is too high)**
- **Interrupt form Mouse (raise interrupt if the mouse is moved or a button is pressed)**
- **Interrupt from Keyboard (raises interrupt when a key is pressed or released)**
- **Interrupt from Hard Disk (raises interrupt when a disk read is completed)**

Which one of these will be handled at the HIGHEST priority?

(a) Interrupt form Hard Disk
(b) Interrupt form Mouse
(c) Interrupt form Keyboard
(d) Interrupt form CPU temperature sensor

GATE 2011

Ans. (d) :

25. **On a non- pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.**

Initialize the address register
Initialize the count to 500
LOOP: Load a byte from device
Store in memory at address given by address register
Increment the a address register
Decrement the count
If count != 0 go to LOOP

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non- load/ store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

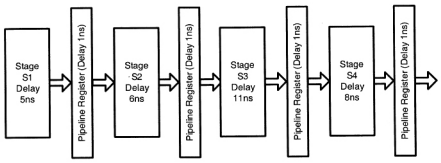
What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?

(a) 3.4 (b) 4.4
(c) 5.1 (d) 6.7

GATE 2011

Ans. (a) :

26. **Consider an instruction pipeline with four stages (S1,S2,S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure**



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

(a) 4.0 (b) 2.5
(c) 1.1 (d) 3.0

GATE 2011

Ans. (b) :

27. **A ROM is used to store the table for multiplication of two 8-Bit unsigned integers. The size of ROM (in bytes) required is**

(a) 256×4 (b) 64 K
(c) $4 K \times 16$ (d) $64 K \times 4$

RPSC Lect. 2011

Ans. (*) :

28. **Addition of two n-bit numbers can generate a number having at most**

(a) n+1 bits (b) n+2 bits
(c) 2n bits (d) n^2 bits

RPSC Lect. 2011

Ans. (a) :

29. **The correct matching for the following pairs is**

a. Activation record	**1. Linking loader**
b. Location counter	**2. Garbage collection**
c. Reference counts	**3. Subroutine call**
d. Address relocation	**4. Assembler**

(a) a – 3, b – 4, c – 1, d – 2
(b) a – 4, b – 3, c – 1, d – 2
(c) a – 4, b – 3, c – 2, d – 1
(d) a – 3, b – 4, c – 2, d – 1

RPSC Lect. 2011

Ans. (d) :

30. Start and stop bits are used in serial communication for
(a) error detection
(b) error correction
(c) synchronization
(d) speeding up communication

RPSC Lect. 2011

Ans. (c) :

31. Consider two cache organizations: the first one is 32 KB 2-way set associative with 32- byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bit in both cases. A 2-to-1 multiplexer has latency of 0.6 ns while a k-bit comparator has a latency of k/10 ns. The hit latency of the set associative organization is h1, while that of the direct mapped one is h2. The value of h1 and h2 will be.
(a) 2.4 ns and 2.3 ns (b) 2.1 ns and 1.3 ns
(c) 1.1 ns and 1.8 ns (d) 1.7 ns and 1.6 ns

RPSC Lect. 2011

Ans. (a) :

32. The addressing mode used in an instruction of the form ADD AX, M is:
(a) direct (b) immediate
(c) indirect (d) index

RPSC Lect. 2011

Ans. (a) :

33. Switching between a supervisor mode and a user mode for a processor is usually done by a
(a) subroutine call (b) branch instruction
(c) software interrupt (d) None of the above

UPPSC LT GRADE 29.07.2018

Ans. (c) :

34. Which one of the following is used to read the control words sequentially from the control memory?
(a) Microprogram address register
(b) Microprogram counter
(c) Control memory address register
(d) Program counter

UPPSC LT GRADE 29.07.2018

Ans. (b) :

35. Which of the following does not have 8 data lines?
(a) 8085 (b) 8086
(c) 8088 (d) Z80

UPPSC LT GRADE 29.07.2018

Ans. (b) :

36. A computer has 32 MB memory. How many bits are needed to access any single byte in the memory?
(a) 25 (b) 16
(c) 24 (d) 20

UPPSC LT GRADE 29.07.2018

Ans. (a) :

37. A computer has 128 MB memory. Each word in this computer is of 8 bytes. How many bits are required to address any single word in the memory?
(a) 27 (b) 24
(c) 23 (d) 25

UPPSC LT GRADE 29.07.2018

Ans. (b) :

38. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit in serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively
(a) 256 MB, 19 bits (b) 256 MB, 28 bits
(c) 512 MB, 20 bits (d) 64 MB, 28 bits

UPPSC LT GRADE 29.07.2018

Ans. (a) :

39. Which of the following is not true regarding registers?
(a) Internal storage of CPU
(b) Can hold either data or instruction
(c) Made up of flip-flip
(d) Cannot store intermediate results

UPPSC LT GRADE 29.07.2018

Ans. (d) :

40. A and B are two 8-bit numbers such that A + B $\leq 2^8$. The number of possible combinations of A and B is
(a) 2^9 (b) 2^8
(c) 2^{16} (d) 2^4-1

UPPSC LT GRADE 29.07.2018

Ans. (c) :

41. Consider a hard disk with a sector size of 512 bytes, and 50 sectors per track. A block may be of several KBs in size. Which of the following is the valid block size?
(a) 256 bytes (b) 786 bytes
(c) 65536 bytes (d) 26112 bytes

BPSC Asstt. Prof. 21.09.2021

Ans. (c) :

42. A computer system has 8 tape drives, with n processes competing for them. Each process may need 4 tape drives. What is the maximum value of n for which the system is guaranteed to be deadlock free?
(a) 2 (b) 3
(c) 4 (d) 1

BPSC Asstt. Prof. 21.09.2021

Ans. (a) :

43. Consider a pipelined processor with the following four stages
IF: Instruction Fetch
ID: Instruction Decode and Operand Fetch
EX: Execute WB: Write Back
The IF, ID and WB stages take one clock cycle each to complete the operation. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX

stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0 R2←R1+R0
MUL R4, R3, R2 R4←R3*R2
SUB R6, R5,R4 R6←R5-R4

(a) 7 (b) 8
(c) 10 (d) 14

ISRO Scientist/Engineer 2009

Ans. (b)

44. Which of the following are macroprocessor pseudo- OPS used for conditional macro expansion?

(i) .DC (ii) .AIF (iii)AGO (iv) .ST

(a) (I), (II),(III) (b) (I),(IV)
(c) (II),(III),(IV) (d) (II),(III)

TRB Poly. Lect. 2017

Ans. (d)

45. Which of the following query processing method is more efficient:

(a) Materialization (b) Tunneling
(c) Serialization (d) Pipelining

TNPSC 2016 (Degree) P-II

Ans. (d) :

46. Consider a paging system with page table stored in memory and with additional associative registers. If 75 percent of all page table reference are found in the associative register, what is the effective memory reference time? Assume the time taken to find a page in associative register is 0.

(a) 400 nanoseconds (b) 300 nanoseconds
(c) 250 nanoseconds (d) 200 nanoseconds

TRB Poly. Lect. 2017

Ans. (*) :

47. Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each cylinder contains 64 sectors (0-63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is < cylinder no., surface no., sector no.>. A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200,9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

(a) 1281 (b) 1282
(c) 1283 (d) 1284

GATE 2013

Ans. (d) :

48. For the 4 block per set associative memory system having 4K blocks, cache memory size is 128 blocks and each block contains 16 words the following parameters are correct

(a) 4 bits Word field, 5 bits set field, 7 bits tag field
(b) 5 bits Word field, 4 bits set field, 7 bits tag field
(c) 5 bits Word field, 7 bits set field, 5 bits tag field
(d) 5 bits Word field, 7 bits set field, 4 bits tag field

RPSC Lect. 2014

Ans. (a) :

49. An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with state latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2)each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EXI, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instruction which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds. Respectively. The value of P/Q is _____.

GATE 2014 (Shift-III)

Ans. 1.50 to 1.60

50. The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

GATE 2014 (Shift-III)

Ans. 1.68 to 1.68

51. Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors, Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one compete rotation. The total time (in milliseconds) needed to read the entire file is.....

GATE 2015 (Shift-I)

Ans. 14020

52. Consider a computer system with DMA support. The DMA module is transferring one 8-bit character in one CPU cycle from a device to memory through cycle stealing at regular intervals. Consider a 2 MHz processor. If 0.5% processor cycles are used for DMA, the data transfer rate of the device is____bits per second.

GATE 2021 (Shift-II)

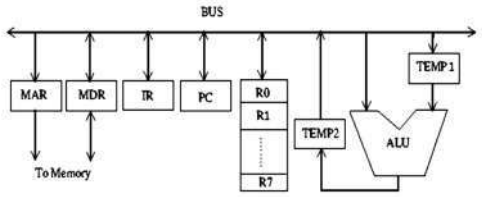
Ans. 80000 to 80000

53. A five-stage pipeline has stage delays of 150, 120, 150, 160 and 140 nanoseconds. The registers that are used between the pipeline stages have a delay of 5 nanoseconds each.
The total time to execute 100 independent instructions on this pipeline, assuming there are no pipeline stalls, is _____ nanoseconds.

GATE 2021 (Shift-I)

Ans. 17160 to 17160

54. Consider the following data path diagram.



Consider an instruction: R0 ← R_1 + R_2. The following steps are used to execute it over the given data path. Assume that PC is inremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_f$, $TEMP1_r$, ALU_{add}, $TEMP2_w$
2. $R1_r$, $TEMP1_w$
3. PC_r, MAR_w, MEM_r
4. $TEMP2_r$, $R0_w$
5. MDR_r, IR_w

Which one of the following is the correct order of execution of the above steps?

(a) 2, 1, 4, 5, 3 (b) 1, 2, 4, 3, 5
(c) 3, 5, 2, 1, 4 (d) 3, 5, 1, 2, 4

GATE 2020

Ans. (c) :

55. A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ration of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

(a) 4.90, 5 (b) 4.76, 5
(c) 3.90, 5 (d) 4.30, 5

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (b) :

56. CPU consist of _____.

(a) ALU and Control Unit
(b) ALU, Control Unit and Monitor
(c) ALU, Control Unit and Hard Disk
(d) ALU, Control Unit and Register

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (d) :

57. Consider an instruction pipeline five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7ns, 10ns,8 ns and 6ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1ns. A program consisting of 12 instructions, I_1,I_2,I_3,…..I_{12} is executed in this pipelined processor. Instruction I_4 is the only branch instruction and its branch target is I_9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

(a) 132 (b) 165
(c) 176 (d) 328

GATE 2013

Ans. (b) :

58. Consider a 5-segment pipeline with a clock cycle time 20ns in each sub operation. Find out the approximate speed-up ratio between pipelined and non-pipelined system to execute 100 instructions. (if an average, every five cycles, a bubble due to data hazard has to be introduced in the pipeline)

(a) 5 (b) 4.03
(c) 4.81 (d) 4.17

ISRO Scientist/Engineer 2020

Ans. (b)

59. Calculate the total time to transmit a 1200 KB file over a link, assuming the one way delay in either direction is 20ms, and no RTT. (Note: 1 KB = 2^{10} bytes, 1 Mbps = 10^6 bits/s). The bandwidth is 1 Mbps, the packet size including the header is 1 KB of which the header is 40 bytes, and the data packets are sent continuously and never lost.

(a) 10 (b) 12
(c) 10.25 (d) 12.52

GPSC Asstt. Manager 13.12.2020 (IT)

Ans. (c) :

60. The action performed by the following command on a new hard disk hd1 in AIX is
chdev -I hd1 -a pv=yes

(a) Makes the disk available for use
(b) Changes the existing pvid on the disk to Yes
(c) Clears volume group locks
(d) Sets the physical volume identifier

GPSC Asstt. Manager 13.12.2020 (IT)

Ans. (d) :

61. Consider an uncompressed stereo audio signal of CD quality which is sampled at 44.1 kHz and quantized using 16 bits. What is required storage space if a compression ratio of 0.5 is achieved for 10 seconds of this audio?

(a) 172 KB (b) 430 KB
(c) 860 KB (d) 1720 KB

ISRO Scientist/Engineer 2015

Ans. (c)

62. The run time mapping from virtual to physical addresses is done by a hardware device called as
(a) Monitor
(b) I/O device
(c) Register
(d) Memory-Management Unit

RPSC VPITI 2018 (IT)

Ans. (d) :

63. Process that periodically checks status of and I/O devices, is known as:
(a) Cold swapping (b) I/O instructions
(c) Polling (d) Dealing

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (c) :

64. Communication between a computer and a keyboard involves_____ transmission.
(a) Simplex (b) Half-Duplex
(c) Automatic (d) Full-Duplex

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (a) :

65. The read access times and the hit ratios for different caches in a memory hierarchy are as given below.

Cache	Read access time (in nanoseconds)	Hit ratio
I-cache	2	0.8
D-cache	2	0.9
L2-cache	8	0.9

The read access time of main memory is 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the write back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is_____.

GATE 2017 (Shift-II)

Ans. 4.72 to 4.72

66. An n-bit microprocessor has:
(a) n-bit program counter
(b) n-bit address register
(c) n-bit ALU
(d) n-bit instruction register
(e) n-bit data register

CGPSC Asstt. Prof. 2014 (Comp. App.)

Ans. (d) :

67. In 8086 the jump condition for the instruction JNBE is?
(a) CF = 0 or 2F = 0
(b) 2F = 0 and SF = 1
(c) CF = 0 and 2F = 0
(d) CF = 0

ISRO Scientist/Engineer 2013

Ans. (c) :

68. In a memory- mapped I/O system which of the following will not be there?
(a) LOAD (b) IN
(c) OUT (d) ADD

TSPSC Manager 2015

Ans. (a) :

69. How many RAM chips of size 8K×16 are required to build 1 Megabyte memory?
(a) 128 (b) 64
(c) 32 (d) 16

TSPSC Manager 2015

Ans. (b) :

70. What is the throughput, if Bus clock is 8.33 MHz, 32 bit-data wide (parallel), synchronous mode?
(a) 269 MBps (b) 267 MBps
(c) 33 MBps (d) 31 MBps

UPSC Poly Lect. 10.03.2019

Ans. (c) :

71. Few addressing modes, fixed instruction size and use more registers for separate memory operations are the features of:
(a) CISC (b) RISC
(c) RAID (d) DMA

UPSC Poly Lect. 10.03.2019

Ans. (b) :

72. The address space of 8086 CPU is
(a) 1 Megabyte (b) 256 Kilobytes
(c) 1 K Megabytes (d) 64 Kilobytes

ISRO Scientist/Engineer 2008

Ans. (a)

73. The TRAP is one of the interrupts available in INTEL 8085. Which one of the following statements is true of TRAP?
(a) It is level triggered
(b) It is negative edge triggered
(c) It is the +ve edge triggered
(d) It is both +ve and - ve edges triggered

ISRO Scientist/Engineer 2008

Ans. (d)

74. An interrupt in which the external device supplies its address as well as the interrupt requests is known as
(a) vectored interrupt
(b) maskable interrupt
(c) non maskable interrupt
(d) designated interrupt

ISRO Scientist/Engineer 2008

Ans. (a)

75. The ability to temporarily halt the CPU and use this time to send information on buses is called
(a) direct memory access
(b) vectoring the interrupt
(c) polling
(d) cycle stealing

ISRO Scientist/Engineer 2008

Ans. (d)

76. The memory Address Register
(a) is a hardware memory device which denotes the location of the current instruction being executed.
(b) is a group of electrical circuit, that performs the intent of instructions fetched from memory
(c) contains the address of the memory location that is to be read from or stored into
(d) contains a copy of the designated memory location specified by the MAR after a "read" or the new contents of the memory prior to a "write"

ISRO Scientist/Engineer 2008

Ans. (c)

77. Which of the following microprocessors does not use microprogramming technique?
(a) Intel 8085 (b) Intel 8086
(c) Intel 80486 (d) Motorola 68040
(e) Motorola 68000

CGPSC Asstt. Prof. 2014 (CS)

Ans. (a)

78. The code which used 7 bits to represent a character is
(a) ASCII (b) BCD
(c) EBCDIC (d) Gray

ISRO Scientist/Engineer 2015

Ans. (a)

79. An 8-bit serial in/serial out shift register is used with a clock frequency of 100 kHz What is the time delay between the serial input and the Q5 output?
(a) 10 μs (b) 50 μs
(c) 60 μs (d) 40 μs

UPPCL AE 2014

Ans. (b) :

80. MOV [BX], AL type of data addressing is called
(a) Register addressing
(b) Immediate addressing
(c) Register indirect addressing
(d) Register relative

ISRO Scientist/Engineer 2011

Ans. (c)

81. Find the memory address of the next instruction executed by the microprocessor (8086), when operated in real mode for CS= 1000 and IP=E000
(a) 10E00 (b) 1E000
(c) F000 (d) 1000E

ISRO Scientist/Engineer 2011

Ans. (*)

82. What is the memory address of fifth element when word size is w?
(a) Address of A[5]=Base(A)+w(5-lower bond)
(b) Address of A[5]=Base(A)=w(5+upper bound)
(c) Address of A[5]=Base(A)+w(6-lower bound)
(d) Address of A[5]=Base(A)+w(6-upper bound)

UPPCL AE 2014

Ans. (a) :

83. There are four bus lines between A and B; and three bus lines between B and C. The number of way a person roundtrip by bus from A to C by way of B will be
(a) 12 (b) 7
(c) 144 (d) 264

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (c) :

84. The example of implied addressing is:
(a) Stack addressing
(b) Indirect addressing
(c) Immediate addressing
(d) None of the above

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (a) :

85. MIMD stands for:
(a) Multiple Instruction Multiple Data
(b) Multiple Instruction Memory Data
(c) Memory Instruction Multiple Data
(d) Multiple Information Memory Data

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (a) :

86. How many address line are needed to address each memory location in a 2048×4 memory chip?
(a) 10 (b) 11
(c) 8 (d) 12

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (b) :

87. Which of the following is not an input device?
(a) Mouse (b) Keyboard
(c) Light Pen (d) VDU

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (d) :

88. Three or more devices share a link in _____ connection.
(a) Unipoint (b) Polarpoint
(c) Point to Point (d) Multipoint

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (d) :

89. A system program that combines the separately compiled modules of a program into a from suitable for execution
(a) assembler
(b) linking loader
(c) cross complier
(d) load and go

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

90. A system contains three programs and each requires three tape units for its operation. The minimum number of tape units which the system must have such that deadlocks never arise is_____
(a) 6 (b) 7
(c) 8 (d) 9

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

91. A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a Translation Look-aside Buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is

(a) 11 bits (b) 13 bits
(c) 15 bits (d) 20 bits

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

92. Computer uses 46- bit virtual address, 32-bit physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second level table (T2). Each entry of T2 stores the base address of a page of the third-level table (T3). Each entry of T3 stores a page Table Entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the size of a page in KB in this computer. ?

(a) 2 (b) 4
(c) 8 (d) 16

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

93. Consider data given in the above question. What is the minimum number of page colours needed to guarantee that no two synonyms map to different sets in the processor cache of this computer ?

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

94. Which access method is used for obtaining a record from cassette tape ?

(a) Direct (b) Sequential
(c) Random (d) Parallel

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

95. The process of converting the analog sample into discrete form is called

(a) Modulation (b) Multiplexing
(c) Quantization
(d) Sampling

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (d) :

96. Which memory is difficult to interface with processor?

(a) Static memory (b) Dynamic memory
(c) ROM (d) None of the option

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

97. For a memory system, the cycle time is

(a) Same as the access time
(b) Longer than the access time
(c) Shorter than the access time
(d) Multiple of the access time

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

98. In comparison with static RAM memory, the dynamic RAM memory has

(a) Lower bit density and higher power consumption
(b) Higher bit density and lower power consumption
(c) Lower bit density and lower power consumption
(d) None of the option

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

99. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4 × 6 array, where each chip is 8K × 4 bits?

(a) 13 (b) 14
(c) 16 (d) 17

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (d) :

100. What is the average Access Time for a Drum rotating at 4000 revolutions per minute?

(a) 2.5 milliseconds (b) 5.0 milliseconds
(c) 7.5 milliseconds (d) 4.0 milliseconds

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

101. The addressing mode used in an instruction of the form ADD X Y, is _____.

(a) Direct (b) Absolute
(c) Indirect (d) Indexed

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (a) :

102. The IETF standard documents are called:

(a) RFC (b) RCF
(c) ID (d) none of the above

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (a) :

103. External Interrupt may not arise becasue of:

(a) Illegal or erroneous use of an instruction
(b) a timing device
(c) external source
(d) I/O devices

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (a) :

104. The Principal of locality of reference justifies the use of:

(a) Non reusable (b) Cache memory
(c) Virtual memory (d) None of the above

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (b) :

105. **Consider a pipelined processor with 5 stages, Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies.**

Consider the following sequence of 8 instructions:

ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL

Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. The Speedup is defined as follows:

$$\text{Speedup} = \frac{\text{Execution time without operand forwarding}}{\text{Execution time with operand forwarding}}$$

The Speedup achieved in executing the given instruction sequence on the pipelined processor (rounded to 2 decimal places) is _____.

GATE 2021 (Shift-II)

Ans. 1.87 to 1.88

106. **Assume a two-level inclusive cache hierarchy, L1 and L2, where L2 is the larger of the two. Consider the following statements.**

S_1 : Read misses in a write through L1 cache do not result in writebacks of dirty lines to the L2.

S_2 : Write allocate policy must be used in conjunction with write through caches and no-write allocate policy is used with writeback caches.

Which of the following statements is correct?

(a) S_1 is true and S_2 is false
(b) S_1 is false and S_2 is true
(c) S_1 is true and S_2 is true
(d) S_1 is false and S_2 is false

GATE 2021 (Shift-II)

Ans. (a) :

107. **Consider a set-associative cache of size 2KB (1 KB = 2^{10} bytes) with cache block size of 64 bytes. Assume that the cache is byte-addressable and a 32-bit address is used for accessing the cache. If the width of the tag field is 22 bits, the associativity of the cache is _____.**

GATE 2021 (Shift-II)

Ans. 2 to 2

108. **Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY[X] denotes the content at the memory location X.**

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	R1 ← MEMORY[5000]	4
MOV R2, (R3)	R2 ← MEMORY[R3]	4
ADD R2, R1	R2 ← R1+R2	2
MOV (R3), R2	MEMORY[R3] ← R2	4
INC R3	R3 ← R3+1	2
DEC R1	R1 ← R1-1	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is _____.

GATE 2021 (Shift-I)

Ans. 50 to 50

109. **Consider a computer system with a byte-addressable primary memory of size 2^{32} bytes. Assume the computer system has a direct-mapped cache of size 32 KB (1 KB = 2^{10} bytes), and each cache block of size 64 bytes.**

The size of the tag field is _____bits.

GATE 2021 (Shift-I)

Ans. 17 to 17

110. **Consider the following two statements.**

S_1 : Destination MAC address of an ARP reply is a broadcast address.

S_2 : Destination MAC address of an ARP request is a broadcast address.

Which one of the following choices is correct?

(a) Both S_1 and S_2 are true.
(b) S_1 is true and S_2 is false.
(c) S_1 is false and S_2 is true.
(d) Both S_1 and S_2 are false.

GATE 2021 (Shift-I)

Ans. (c) :

111. **Consider a database implemented using B+ tree for file indexing and installed on a disk drive with block size of 4 KB. The size of search key is 12 bytes and the size of tree/disk pointer is 8 bytes. Assume that the database has one million records. Also assume that no node of the B+ tree and no records are present initially in main memory. Consider that each record fits into one disk block. The minimum number of disk accesses required to retrieve any record in the database is _____.**

GATE 2020

Ans. 4 to 4

112. Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5-stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the pipelined processor over the non-pipelined processor (round off to 2 decimal places) is _____.

GATE 2020

Ans. 2.15 to 2.18

113. A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immeidate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is _____.

GATE 2020

Ans. 14 to 14

114. Consider the following five disk access requests of the form (request id, cylinder number) that are present in the disk scheduler queue at a given time.
(P, 155), (Q, 85), (R, 110), (S, 30), (T, 115)
Assume the head is positioned at cylinder 100. The scheduler follows Shortest Seek Time First scheduling to service the requests.
Which one of the following statements is FALSE?
(a) T is serviced before P.
(b) Q is serviced after S, but before T.
(c) The head reverses its direction of movement between servicing of Q and P.
(d) R is serviced before P.

GATE 2020

Ans. (b) :

115. Consider three registers R1, R2 and R3 that store numbers in IEEE-754 single precision floating point format. Assume that R1 and R2 contain the values (in hexadecimal notation) 0x42200000 and 0xC1200000, respectively.
If R3 = $\frac{R1}{R2}$, what is the value stored in R3?
(a) 0x40800000 (b) 0xC0800000
(c) 0x83400000 (d) 0xC8500000

GATE 2020

Ans. (b) :

116. A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.
A1 = 0x42C8A4, A2 = 0x546888,
A3=0x6A289C, A4 = 0x5E4880
Which one of the following is TRUE?
(a) A1 and A4 are mapped to different cache sets.
(b) A2 and A3 are mapped to the same cache set.
(c) A3 and A4 are mapped to the same cache set.
(d) A1 and A3 are mapped to the same cache set.

GATE 2020

Ans. (b) :

117. A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____.

GATE 2020

Ans. 13.5 to 13.5

118. Consider the following statements.
I. Daisy chaining is used to assign priorities in attending interrupts.
II. When a device raises a vectored interrupt the CPU does polling to identify the source of interrupt.
III. In polling, the CPU periodically checks the status bits to know if any device needs its attention.
IV. During DMA, both the CPU and DMA controller can be bus masters at the same time.
Which of the above statements is/are TRUE?
(a) I and II only (b) I and IV only
(c) I and III only (d) III only

GATE 2020

Ans. (c) :

119. Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is_____.

GATE 2017 (Shift-II)

Ans. 18.0 to 18.0

120. In a two-level cache system, the access times of L_1 and L_2 caches are 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2. The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are:
(a) 0.111 and 0.056
(b) 0.056 and 0.111

(c) 0.0892 and 0.1784
(d) 0.1784 and 0.0892

GATE 2017 (Shift-II)

Ans. (a) :

121. Which of the following is/are shared by all the threads in a process?
I. Program counter
II. Stack
III. Address space
IV. Registers
(a) I and II only (b) III only
(c) IV only (d) III and IV only

GATE 2017 (Shift-II)

Ans. (b) :

122. In a file allocation system, which of the following allocation scheme(s) can be used if no external fragmentation is allowed?
I. Contiguous
II. Linked
III. Indexed
(a) I and III only (b) II only
(c) III only (d) II and III only

GATE 2017 (Shift-II)

Ans. (d) :

123. Match the following:

(P) static char var;	(i) Sequence of memory locations to store addresses
(Q) m = malloc (10); m = NULL;	(ii) A variable located in data section of memory
(R) char *ptr[10];	(iii) Request to allocate a CPU register to store data
(S) register int varl;	(iv) A lost memory which cannot be freed

(a) P → (ii), Q → (iv), R → (i), S → (iii)
(b) P → (ii), Q → (i), R → (iv), S → (iii)
(c) P → (ii), Q → (iv), R → (iii), S → (i)
(d) P → (iii), Q → (iv), R → (i), S → (ii)

GATE 2017 (Shift-II)

Ans. (a) :

124. Consider the following reservation table for a pipeline having three stages S1,S2 and S3.

Time→

	1	2	3	4	5
S1	X				X
S2		X		X	
S3			X		

The minimum average latency (MAL) is_____

GATE 2015 (Shift-III)

Ans. 3

125. Consider the following code sequence having five instructions I_1 to I_5. Each of these instructions has the following format.
OP RI, Rj, Rk
Where operation OP is performed on content of registers Rj and Rk and the result is stored in register Ri.
I1: ADD R1, R2, R3
I2: MUL R7, R1, R3
I3: SUB R4, R1, R5
I4: ADD, R3, R2, R4
I5: MUL R7, R8, R9
Consider the following three statements.
S1: There is an anti-dependence between instruction I_2 and I_5
S2: There is an anti-dependence between instructions I_2 and I_4
S3: Within an instruction pipeline an anti-dependence always creates one or more stalls.
Which one of above statements is/are correct?
(a) only S1 is true
(b) only S2 is true
(c) only S1 and S3 are true
(d) only S2 and S3 are true

GATE 2015 (Shift-III)

Ans. (b) :

126. Consider a machine with a byte addressable main memory of 2^{20} bytes, block size of 16 bytes and a direct mapped cache having 2^{12} cache lines. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$. What are the tag and cache line address (in hex) for main memory address $(E201F)_{16}$?
(a) E, 201 (b) F, 201
(c) E, E20 (d) 2, 01F

GATE 2015 (Shift-III)

Ans. (a) :

127. The maximum number of processes that can be in ready state for a computer system with n CPUs is
(a) n (b) n^2
(c) 2^n (d) Independent of n

GATE 2015 (Shift-III)

Ans. (d) :

128. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline, The speed up achieved in this pipelined processor is.....

GATE 2015 (Shift-I)

Ans. 3.2

129. Consider a 4-bit Johnson counter with an initial Value of 0000. The counting sequence of this counter is
(a) 0, 1, 3, 7, 15, 14, 12, 8, 0
(b) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
(c) 0, 2, 4, 6, 8, 10, 12, 14, 0
(d) 0, 8, 12, 14, 15, 7, 3, 1, 0

GATE 2015 (Shift-I)

Ans. (d) :

130. Consider a system with byte-addressable memory, 32-bit logical address, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in megabytes is.....

GATE 2015 (Shift-I)

Ans. 4

131. For computers based on three-address instruction formats, each address field can be used to specify which of the following:

(S1) A memory operand
(S2) A processor register
(S3) An implied accumulation register

(a) Either S1 or S2 (b) Either S2 or S3
(c) Only S2 and S3 (d) All of S1, S2 and S3

GATE 2015 (Shift-I)

Ans. (a) :

132. Consider a main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is _____ .

GATE 2014 (Shift-II)

Ans. 10000 to 10000

133. In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context ?

(a) A smaller block size implies spatial locality
(b) A smaller block size implies a smaller cache tag and hence lower cache tag overhead
(c) A smaller block size implies a larger cache tag and hence lower cache hit time
(d) A smaller block size incurs a lower cache miss penalty

GATE 2014 (Shift-II)

Ans. (d) :

134. If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected ?

(a) Width of tag comparator
(b) Width of set index decoder
(c) Width of way selection multiplexor
(d) Width of processor to main memory data bus

GATE 2014 (Shift-II)

Ans. (d) :

135. A FAT (file allocation table) based file system is being used and the total overhead of each entry in the FAT is 4 bytes in size. Given a 100×10^6 bytes disk on which the file system is stored and data block size is 10^3 bytes, the maximum size of a file that can be stored on this disk in units of 10^6 bytes is _____.

GATE 2014 (Shift-II)

Ans. 99.55 to 99.65

136. Let $k = 2_n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to a

(a) k-bit binary up counter
(b) k-bit binary down counter.
(c) k-bit ring counter.
(d) k-bit Johnson counter

GATE 2014 (Shift-II)

Ans. (c) :

137. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is ___

GATE 2014 (Shift-II)

Ans. 20 to 20

Statement for linked answer question 138 and 139.

A computer has a 256 Kbyte, 4-way set associative, write back data cache with block size of 32 Byte. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

138. The number of bits in the tag field of an address is

(a) 11 (b) 14
(c) 16 (d) 27

GATE 2012

Ans. (c) :

139. The size of the cache tag directory is

(a) 160 Kbits (b) 136 Kbits
(c) 40 Kbits (d) 32 Kbits

GATE 2012

Ans. (a) :

140. A file system with 300 GByte disk uses a file descriptor with 8 direct block addresses, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. The maximum possible file size in this file system is

(a) 3 KBytes
(b) 35 KBytes
(c) 280 KByes
(d) Dependent on the size of the disk

GATE 2012

Ans. (b) :

141. Register renaming is done in pipelined processor
(a) as an alternative to register allocation at compile time
(b) for efficient access to function parameters and local variables
(c) to handle certain kinds of hazards
(d) as part of address translation
GATE 2012

Ans. (c) :

142. 8085 include auxiliary carry flag as _____flag
(a) Third (b) Fourth
(c) Fifth (d) Sixth
MPPSC State Forest Service Examination 2014

Ans. (c) :

143. EEPROM can be erased by exposing it to
(a) Magnetic field (b) Electric charge
(c) Sun Light (d) Ultraviolet radiation
MPPSC State Forest Service Examination 2014

Ans. (b) :

144. In 8085, two buffer registers are
(a) Instruction Register, accumulator
(b) Address buffer, Address data buffer
(c) Address buffer, Instruction Register
(d) DAA, address data register
MPPSC State Forest Service Examination 2014

Ans. (b) :

145. _____ is used for storing programs that are not be changed
(a) ROM (b) RAM
(c) Monitor (d) Cache Memory
MPPSC State Forest Service Examination 2014

Ans. (a) :

146. Which of the following memory is refreshed a number of times per second?
(a) Hard disk (b) RAM
(c) ROM (d) Dynamic RAM
MPPSC State Forest Service Examination 2014

Ans. (d) :

147. Time taken to position the Read/Write head at the desired track of disk is known as
(a) Access time (b) Seek time
(c) Latency time (d) Data transfer time
MPPSC State Forest Service Examination 2014

Ans. (b) :

148. Which of the following symbols are used in Assembly language?
(a) Tags (b) Numbers
(c) Characters (d) Mnemonics
MPPSC State Forest Service Examination 2014

Ans. (d) :

149. DMA controller is used is a computer to transfer the data
(a) From main memory to CUP
(b) From hard disk to main memory
(c) From ROM to RAM
(d) All options are correct
MPPSC State Forest Service Examination 2014

Ans. (b) :

150. _____ system software that converts assembly language program to machine language
(a) Compiler (b) Interpreter
(c) Assembler (d) Loader
MPPSC State Forest Service Examination 2014

Ans. (c) :

151. Frame buffer is termed as
(a) Virtual Memory (b) ROM
(c) I/O Buffer (d) Video Memory
MPPSC State Forest Service Examination 2014

Ans. (d) :

152. Consider a system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10 ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?
(a) 13.0 ns (b) 12.8 ns
(c) 12.6 ns (d) 12.4 ns
ISRO Scientist/Engineer 2016 (July)

Ans. (c) :

153. A CPU generates 32- bit virtual addresses. The page size is 4 KB. The processor has a translation look- aside buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is
(a) 11 bits (b) 13 bits
(c) 15 bits (d) 20 bits
ISRO Scientist/Engineer 2016 (July)

Ans. (c) :

154. Relative mode of addressing is most relevant to writing
(a) Co- routines
(b) Position- independent code
(c) Sharable code
(d) Interrupt Handlers
ISRO Scientist/Engineer 2016 (July)

Ans. (b) :

155. Register renaming is done in pipelined processors
(a) As an alternative to register allocation at compile time
(b) For efficient access to function parameters and local variables
(c) To eliminate certain kind of hazards
(d) As part of address translations
ISRO Scientist/Engineer 2016 (July)

Ans. (c) :

156. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial fashion in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk respectively.
(a) 256 MB, 19 bits (b) 256 MB, 28 bits
(c) 512 MB, 20 bits (d) 64 GB, 28 bits
ISRO Scientist/Engineer 2016 (July)

Ans. (a) :

157. Consider a non- pipelined processor with a clock rate of 2.5 GHz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 GHz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is

(a) 3.2 (b) 3.0
(c) 2.2 (d) 2.0

ISRO Scientist/Engineer 2016 (July)

Ans. (a) :

158. In a system having a single processor, a new process arrives at the rate of six processes per minute and each such process requires seven seconds of service time. What is the CPU utilization?

(a) 70% (b) 30%
(c) 60% (d) 64%

ISRO Scientist/Engineer 2011

Ans. (a)

159. Number of chips (128× 8 RAM) needed to provide a memory capacity of 2048 bytes

(a) 2 (b) 4
(c) 8 (d) 16

ISRO Scientist/Engineer 2011

Ans. (d)

160. Consider a 32-bit machine where four-level paging scheme is used. If the hit ratio to TLB is 98% and it takes 20 nanoseconds to search the TLB and 100 nanoseconds to access the main memory what is effective memory access time in nanoseconds?

(a) 126 (b) 128
(c) 122 (d) 120

ISRO Scientist/Engineer 2011

Ans. (b)

161. Data is transmitted continuously at 2.048 Mbps rate for 10 hours and received 512 bit errors. What is the bit error rate?

(a) 6.9 e-9 (b) 6.9 e-6
(c) 69 e-9 (d) 4 e-9

ISRO Scientist/Engineer 2011

Ans. (a)

162. Warnier Diagram enables the analyst to represent

(a) Class Structure
(b) Information Hierarchy
(c) Data Flow
(d) State Transition

ISRO Scientist/Engineer 2011

Ans. (b)

163. If a microcomputer operates at 5 MHz with an 8-bit bus and a newer version operates at 20MHz with a 32-bit bus, the maximum speed-up possible approximately will be

(a) 2 (b) 4
(c) 8 (d) 16

ISRO Scientist/Engineer 2011

Ans. (b)

164. A fast wide SCSI-II disk drive spins at 7200 RPM, has a sector size of 512 bytes, and holds 160 sectors per track. Estimate the sustained transfer rate of this drive.

(a) 576000 Kilobytes/sec
(b) 9600 Kilobytes/sec
(c) 4800 Kilobytes /sec
(d) 19200 Kilobytes/sec

ISRO Scientist/Engineer 2011

Ans. (b)

165. What is the meaning of $\overline{RD}$ signal in Intel 8151A?

(a) Read (When it is low)
(b) Read (when it is high)
(c) Write (when it is low)
(d) Read and write (When it is high)

ISRO Scientist/Engineer 2011

Ans. (a)

166. Consider a direct mapped cache with 64 blocks and a block size of 16 bytes. To what block number does the byte address 1206 map to?

(a) Does not map (b) 6
(c) 11 (d) 54

ISRO Scientist/Engineer 2011

Ans. (c)

167. On receiving an interrupt from an I/O device, the CPU

(a) Halts for a predetermined time
(b) Branches off to the interrupt service routine after completion of the current instruction
(c) Branches off to the interrupt service routine immediately
(d) Hands over control of address bus and data bus to the interrupting device

ISRO Scientist/Engineer 2009

Ans. (a)

168. Compared to CISC processors, RISC processors contain;

(a) more register and smaller instruction set
(b) larger instruction set and less registers
(c) less registers and smaller instruction set
(d) more transistor elements

ISRO Scientist/Engineer 2009

Ans. (c)

169. Which of the following is/are true of the auto increment addressing mode?

1. It is useful in creating self relocating code
2. If it is included in an instruction set architecture, then an additional ALU is required for effective address calculation
3. The amount of increment depends on the size of the data item accessed

(a) 1 only (b) 2 only
(c) 3 only (d) 2 and 3 only

ISRO Scientist/Engineer 2009

Ans. (c)

170. Which of the flowing statements about relative addressing mode is FALSE?
(a) It enables reduced instruction size
(b) It allows indexing of array element with same instruction
(c) It enables easy relocation of data
(d) It enables faster address calculation than absolute addressing

ISRO Scientist/Engineer 2009

Ans. (b)

171. The use of multiple register windows with overlap causes a reduction in the number of memory accesses for
1. Function locals and parameters
2. Register saves and restores
3. Instruction fetches
(a) 1 only (b) 2 only
(c) 3 only (d) 1,2 and 3

ISRO Scientist/Engineer 2009

Ans. (b)

172. A processor that has carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be
(a) 1, 1, 0 (b) 1, 0, 0
(c) 0, 1, 0 (d) 1, 0, 1

ISRO Scientist/Engineer 2009

Ans. (b)

173. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX. How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?
(a) 10,3,1024 (b) 8,5,256
(c) 5,8,2048 (d) 10,3,512

ISRO Scientist/Engineer 2009

Ans. (a)

174. A CPU has 24-bit instruction. A program starts at address 300 (in decimal). which one of the following is a legal program counter (all values in decimal)?
(a) 400 (b) 500
(c) 600 (d) 700

ISRO Scientist/Engineer 2009

Ans. (c)

175. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stores in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively
(a) 256 Mbyte, 19 bits
(b) 256 Mbyte, 28 bits
(c) 512 Mbyte, 20 bits
(d) 64 Gbyte, 28 bits

ISRO Scientist/Engineer 2009

Ans. (b)

176. In which addressing mode, the effectives address of the operand is generated by adding a constant value to the content of a register?
(a) Absolute mode (b) Indirect mode
(c) Immediate mode (d) Index mode

ISRO Scientist/Engineer 2009

Ans. (d)

177. A certain microprocessor requires 4.5 microseconds to respond to an interrupt. Assuming that the three interrupts I_1, I_2 and I_3 require the following execution time after the interrupt is recognized:
(i) I_1 requires 25 micro seconds
(ii) I_2 requires 35 micro seconds
(iii) I_3 requires 20 micro seconds
I_1 has the highest priority and I_3 has the lowest. What is the possible range of time for I_3 to be executed assuming that it may or may not occur simultaneously with other interrupts?
(a) 24.5 microseconds to 39.5 microseconds
(b) 24.5 microseconds to 93.5 microseconds
(c) 4.5 microseconds to 24.5 microseconds
(d) 29.5 microseconds to 93.5 microseconds

ISRO Scientist/Engineer 2009

Ans. (b)

178. The process of organizing the memory into two banks to allow 8 and 16- bit data operation is called
(a) Bank switching
(b) Indexed mapping
(c) Two- way memory interleaving
(d) Memory segmentation

ISRO Scientist/Engineer 2009

Ans. (c)

179. Using a larger block size in a fixed block size file system leads to
(a) Better disk throughput but poorer disk space utilization
(b) Better disk throughput and better disk space utilization
(c) Poorer disk throughput but better disk space utilization
(d) Poorer disk throughput and poorer disk space utilization

ISRO Scientist/Engineer 2009

Ans. (a)

180. How many 128×8 bit RAM is are required to design 32K×32 bit RAM?
(a) 512 (b) 1024
(c) 128 (d) 32

ISRO Scientist/Engineer 2017 (May)

Ans. (b) :

181. The most appropriate matching for the following pairs :

X **: Indirect Addressing**	**1. Loop**
Y **: Immediate Addressing**	**2. Pointers**
Z **: Auto Decrement Addressing**	**3.Constants**

(a) *X*-3, *Y*-2, *Z*-1 (b) *X*-2, *Y*-3, *Z*-1
(c) *X*-3, *Y*-1, *Z*-2 (d) *X*-2, *Y*-1, *Z*-3

ISRO Scientist/Engineer 2017 (May)

Ans. (b) :

182. Which interrupt in 8085 Microprocessor is unmaskable?

(a) RST 5.5 (b) RST 7.5
(c) TRAP (d) Both (a) and (b)

ISRO Scientist/Engineer 2017 (May)

Ans. (c) :

183. A cache memory needs an access time of 30 ns and main memory 150 ns, what is the average access time of CPU (assume hit ratio= 80%)?

(a) 60 ns (b) 30 ns
(c) 150 ns (d) 70 ns

ISRO Scientist/Engineer 2017 (May)

Ans. (a) :

184. What does the data dictionary identify?

(a) Field names (b) Field formats
(c) Field Types (d) All of these

ISRO Scientist/Engineer 2017 (May)

Ans. (d) :

185. Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50×10^6 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512-byte sector of the disk is _____ .

GATE 2015 (Shift-II)

Ans. 6.1 to 6.2

186. A computer system implements 8 kilobytes pages and a 32-bit physical address space. Each page table entry contains a valid but, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the virtual address supported by the system is _____ bits.

GATE 2015 (Shift-II)

Ans. 36

187. Consider the sequence of machine instructions given below:

```
MUL   R5, R0, R1
DIV   R6, R2, R3
ADD   R7, R5, R6
SUB   R8, R7, R4
```

In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages. (1) Instruction Fetch and Decode (IF), OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instructions is _____ .

GATE 2015 (Shift-II)

Ans. 13

188. Consider a processor with byte-addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word (PSW) are of size 2 bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- **Store the current value of PC in the stack.**
- **Store the value of PSW register in the stack**
- **Load the starting address of the subroutine in PC.**

The content of PC just before the fetch of a CALL instruction is $(SFA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is

(a) $(016A)_{16}$ (b) $(016C)_{16}$
(c) $(0170)_{16}$ (d) $(0172)_{16}$

GATE 2015 (Shift-II)

Ans. (d) :

189. Consider six memory partitions of sizes 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB, where KB refers to kilobyte. These partitions need to be allotted to four processes of sizes 357 KB, 210 KB, 468 KB and 491 KB in that order. If the best fit algorithm is used, which partitions are NOT allotted to any process ?

(a) 200 KB and 300 KB
(b) 200 KB and 250 KB
(c) 250 KB and 300 KB
(d) 300 KB and 400 KB

GATE 2015 (Shift-II)

Ans. (a) :

190. A computer system implements a 40-bit virtual address, page size of 8 kilobytes, and a 128-entry translation look-aside buffer (TLB) organized into 32 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____ .

GATE 2015 (Shift-II)

Ans. 22

191. A RAM chip has a capacity of 1024 words of 8 bits each (1K× 8). The number of 2× 4 decoders with enable line needed to construct a 16K× 16 RAM from 1K × 8 RAM is

(a) 4 (b) 5
(c) 6 (d) 7

GATE 2013

Ans. (b) :

192. In a k- way set associative cache, the cache is divided into v sets, each of which consists of K lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (S+1). The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from

(a) (j mod v)* k to (j mode v) * k+ (k-1)
(b) (j mod v)to (j mode v) + (k-1)
(c) (j mod k) to (j mode k) + (v-1)
(d) (j mod k)* v to (j mode k) * v+ (v-1)

GATE 2013

Ans. (a) :

193. Which of the following is not TRUE for storage compaction?

(a) Technique of storage compaction involves moving all occupied areas of storage to one end or other of main storage
(b) compaction does not involve relocation of programs
(c) compaction is also know as garbage collection
(d) the system must stop everything while it performs the compaction

RPSC VPITI 2014 (IT)

Ans. (b) :

194. At any given point of time, while a program is executing, a number of elements together characterizes the program uniquely. These elements are stored in a data structure called

(a) Program Counter (b) Stack
(c) Heap (d) Process Control Block

RPSC VPITI 2014 (IT)

Ans. (d) :

195. Which is not a valid activity for causing transition of a process state?

(a) Release (b) Exit
(c) Dispatch (d) Time-out

RPSC VPITI 2014 (IT)

Ans. (b) :

196. Under which of the following situations, a process will be switched?

(a) Clock interrupt (b) 1/O Interrupt
(c) Memory Fault (d) All the above

RPSC VPITI 2014 (IT)

Ans. (d) :

197. Which of the following refers to the associative memory?

(a) The address of the data is generated by the CPU
(b) The address of the data is supplied by the users
(c) there is no need for an address i.e. the data is used as an address
(d) The data are accessed sequentially

RPSC VPITI 2014 (IT)

Ans. (c) :

198. A system program that combines the separately compiled modules of a program into a form suitable for execution

(a) assembler (b) linker
(c) compiler (d) Parser

RPSC VPITI 2014 (IT)

Ans. (b) :

199. Message passing system allows processes to:

(a) share data
(b) communicate with one another without resorting to shared data.
(c) Synchronize with one another without resorting to shared data.
(d) communicate with one another by resorting to shared data

RPSC VPITI 2014 (IT)

Ans. (b) :

200. Which of the following is/ are true with respect to "Photonics" (a) It's a science of light generation, detection and manipulation (b) It will exploit high-speed silicon photonics to improve data transfer between core and memory exponentially (c) It would exponentially improve the power of microprocessor (d) It will replace the copper wire connectivity in processors.

(a) Only a (b) a, b, and c
(c) a and d (d) all of them

RPSC VPITI 2014 (IT)

Ans. (*) :

201. Which of the following is hardware interrupts?

(a) RST 5.5, RST 6.5, RST 7.5
(b) INTR
(c) TRAP
(d) All of the above

RPSC Lect. 2014

Ans. (d) :

202. The RS 232. ports are commonly used for communication between two devices within 50 to 100 feets. Which of the following statement is incorrect related to RS 232 :

(a) Maximum data rate is 20,000 bits per second
(b) It uses unbalanced lines
(c) Allows communication between two devices only
(d) 8051 does not support RS 232 ports directly

RPSC Lect. 2014

Ans. (*) :

203. Which addressing mode is not supported by 8051 microcontroller

(a) Register addressing
(b) Direct addressing

(c) Register relative addressing
(d) Relative base index addressing

RPSC Lect. 2014

Ans. (d) :

204. Which 8051μ-Controller instruction is incorrect
(a) MOV R4,#11h (b) MOV B,#11
(c) MOV R4, R7 (d) MOV 56h,A

RPSC Lect. 2014

Ans. (c) :

205. Which statement is incorrect related to the 8051 I/O Ports
(a) Ports P1, P2, and P3 have internal pullups
(b) Ports P1, P2, P3 can support up to 12 LS-TTL inputs
(c) Port 0 has open drain outputs
(d) Port 0 internal pullups are not active during normal port operation

RPSC Lect. 2014

Ans. (d) :

206. Which is false statement for the 8051 microcontroller architecture
(a) it contains internal RAM of 128 Bytes
(b) It has 16 bit program counter (PC) and data pointer (DPTR)
(c) It contains one 16- bit timer/counters
(d) It has 2 external and 3 internal interrupt sources

RPSC Lect. 2014

Ans. (c) :

207. Each interrupt has a specific place in code memory where program execute. The correct sequence of 8051μ Controller interrupt increasing order vector address is:

Type of Interrupt
A. External Interrupt 0
B. Timer 0 overflow
C. External Interrupt 1
D. Timer 1 overflow

(a) A, B, C, D (b) B, D, A, C,
(c) A, C, B, D, (d) D, C, B, A

RPSC Lect. 2014

Ans. (a) :

208. MIMD is used employed to achieve-
(a) computation (b) parallelism
(c) pipelining (d) distribution

RPSC Lect. 2014

Ans. (b) :

209. A memory of 1000K has what amount of user space if size of OS is 200K, and loader consumes 50 K?
(a) 800 K (b) 950 K
(c) 750 K (d) 1150 K

RPSC Lect. 2014

Ans. (a) :

210. Which of the following factors do not affect the hit ratio of the cache?
(a) Block replacement algorithm
(b) Block frame size
(c) Cycle count
(d) Main memory size

RPSC Lect. 2014

Ans. (*) :

211. The most appropriate matching for following pairs is

X. Indirect addressing	**1. Loop**
Y. Auto decrement addressing	**2. Constraints**
Z. Immediate addressing	**3. Pointers**

(a) X-1, Y-3, Z-2 (b) X-3, Y-1, Z-2
(c) X-2, Y-1,Z-3 (d) X-3, Y-2,Z-1

RPSC Lect. 2014

Ans. (b) :

212. How many address line and I/O lines are required? If capacity of RAM is 1024 words of 8-bits.
(a) 10 bit address line and 8 bit I/O lines
(b) 8 bit address line and 10 bit I/O line
(c) 10 bit address line and 10 bit I/O line
(d) None of the above

RPSC Lect. 2014

Ans. (a) :

213. On a system using fixed partitions with sizes 2^{16}, 2^{24} and 2^{32}. How many bits must the limit register have?
(a) 8 bits (b) 16 bits
(c) 24 bits (d) 32 bits

RPSC VPITI 2018 (IT)

Ans. (d) :

214. What is the minimum size of ROM required to store the complete truth table of an 8 bit* 8 bit multiplier?
(a) 64 k × 16 bits (b) 32 k × 16 bits
(c) 16 k × 32 bits (d) 64 k × 32 bits

RPSC VPITI 2018 (IT)

Ans. (a) :

215. The principle of locality of reference is related to
(a) DMA (b) Polling
(c) Cache Memory (d) None

RPSC VPITI 2018 (IT)

Ans. (c) :

216. Which function is used to map the contents of the memory to the cache memory?
(a) Assign function
(b) Construction function
(c) Mapping function
(d) None of the mentioned

RPSC VPITI 2018 (IT)

Ans. (c) :

217. A CPU has 16 bit program counter. This means that the CPU can address.
(a) 16k memory location
(b) 32 k memory location
(c) 64 k memory location
(d) 256 k memory location

RPSC VPITI 2018 (IT)

Ans. (c) :

218. Match the following according to cloud computing stack:

(1) SaaS	(A) Accessed by web browser
(2) PaaS	(B) Accessed by cloud development environment
(3) IaaS	(C) Accessed by virtual infrastructure manager

(a) 1–A, 2–B, 3–C (b) 1–C, 2–B. 3–A
(c) 1–B, 2–A, 3–C (d) 1–A, 2–C, 3–B

TNPSC 2016 (Degree) P-II

Ans. (a) :

219. Block size in GFS is normally:
(a) 4 KB (b) 16 KB
(c) 64 MB (d) 128 MB

TNPSC 2016 (Degree) P-II

Ans. (c) :

220. Multi core CPU is ..... efficient compared to many core GPU in cloud data centers in term of computational speed and energy consumption.
(a) Less (b) More
(c) Equally (d) Not comparable

TNPSC 2016 (Degree) P-II

Ans. (a) :

221. Application frameworks provide a means for creating ..... hosted application using IDE.
(a) PaaS (b) SaaS
(c) CaaS (d) laaS

TNPSC 2016 (Degree) P-II

Ans. (b) :

222. Which kind of mapping is provided to get logical data independence:
(a) Conceptual to internal level
(b) External to conceptual level
(c) Conceptual to external
(d) Internal to conceptual

TNPSC 2016 (Degree) P-II

Ans. (b) :

223. In a tightly coupled symmetric multiprocessor system, processes communicate of each other by means of:
(a) Message passing (b) Shared memory
(c) Distributed memory (d) Cache memory

TNPSC 2016 (Degree) P-II

Ans. (b) :

224. Contents of which fields of Program Status Word (PSW) define the subsequent actions of the CPU:
(a) Condition code, privileged mode, program counter
(b) Condition code, privileged mode, interrupt mask
(c) Privileged mode, interrupt mask, interrupt code
(d) Privileged mode, interrupt mask, program counter

TNPSC 2016 (Degree) P-II

Ans. (d) :

225. In the Pentium virtual memory, Local Descriptor Table (LDT) and Global Descriptor Table (GDT) are used:
Which of the following is correct?
(i) There is a LDT for each program and a single GDT shared by all programs in the computer
(ii) LDT describes system segments, GDT describes segments of program
(a) (i) is true, (ii) is true
(b) (i) is true, (ii) is false
(c) (i) is false, (ii) is true
(d) (i) is false, (ii) is false

TNPSC 2016 (Degree) P-II

Ans. (b) :

226. The total time to prepare a disk drive mechanism for a block of data to be read from is its:
(a) Access time
(b) Seek time
(c) Latency plus seek time
(d) Access time plus seek time plus transmission time

TNPSC 2016 (Degree) P-II

Ans. (c) :

227. Block or buffer caches are used:
(a) To improve disk performance
(b) To handle interrupts
(c) To increase the capacity of main memory
(d) To speed up main memory read operation

TNPSC 2016 (Degree) P-II

Ans. (a) :

228. If T_1 and T_2 are average access times of upper level memory M1 and lower level memory M2 in a 2- level memory hierarchy and H is the hit rate in M1, then the overall average access time is given by _____ assuming that in case of a miss in M1, a block is first copied from M2 to M1 and then accessed from M1:
(a) $T_1 + (1-H) \times T_2$ (b) $(1-H) \times T_1 + T_2$
(c) $(T_1 + T_2)(1-H)$ (d) $(T_1 + T_2)(1+H)$

TRB Poly. Lect. 2017

Ans. (a)

229. Let A=69, and B=90.If A and B are unsigned decimal 8- bit integers, then A–B will result in_____ and if A and B are sign and magnitude 8- bit integers, then A+B will result in_____
(a) overflow, overflow
(b) overflow, correct result
(c) correct result, underflow
(d) underflow, overflow

TRB Poly. Lect. 2017

Ans. (d)

230. Construct the state table of a mod- 4 up/ down counter that detects the count of 2:

(A)

Present State	Next state		Output z	
	x=0	x=1	x=0	x=1
S_0	S_1	S_2	0	0
S_1	S_2	S_1	0	0
S_2	S_3	S_0	1	1
S_3	S_0	S_3	0	0

(B)

Present State	Next state		Output z	
	x=0	x=1	x=0	x=1
S_0	S_0	S_3	0	0
S_1	S_3	S_0	1	0
S_2	S_2	S_1	0	1
S_3	S_1	S_2	0	0

(C)

Present State	Next state		Output z	
	x=0	x=1	x=0	x=1
S_0	S_1	S_3	0	0
S_1	S_2	S_0	0	0
S_2	S_3	S_1	1	1
S_3	S_0	S_2	0	0

(D)

Present State	Next state		Output z	
	x=0	x=1	x=0	x=1
S_0	S_1	S_1	0	1
S_1	S_3	S_2	0	0
S_2	S_2	S_0	1	1
S_3	S_0	S_3	0	0

TRB Poly. Lect. 2017

Ans. (c)

231. The Booth technique for recording multiply of +13 and – 6[01101 and 11010] is :

(a) 1110 0011 01 (b) 1110 1100 10
(c) 1110 1010 10 (d) 1110 0011 00

TRB Poly. Lect. 2017

Ans. (b)

232. MFLOPS can be abbreviate as:

(a) Millions of Floating-Point operations performed per second.
(b) Millions of Fixed-Length operations performed per second.
(c) Millions of Floating-Limited operations performed per second.
(d) Millions of Fixed-Limited operations performed per second.

TRB Poly. Lect. 2017

Ans. (a)

233. An SD RAM has 8K rows, with an access time of 4 clock cycles for each row, and a refresh period of 64 ms. If the clock rate is 133 MHz, the refresh overhead will be:

(a) 0.0038 (b) 0.246
(c) 0.68 (d) 4.35

TRB Poly. Lect. 2017

Ans. (a)

234. Suppose a counter has three states namely Q_0, Q_1 and Q_3. Their levels may be 0 to 1, 0 to 1 and 1 to 0 respectively. If a positive edge will change the state of Q_0 from 1 to 0, which will force Q_1 from 1 to 0 and Q_3 from 0 to 1. Determine what type of counter have this effect.

(a) Johnson Counters (b) Ripple counters
(c) UP Counters (d) Down Counters

TRB Poly. Lect. 2017

Ans. (b)

235. Address decoding in large sized memory chips is by means of row and column decoding rather than flat decoding because:

(a) decoders decode the input address
(b) decoders have priorities built-in
(c) the size of the flat decoder becomes very large
(d) row and column decoders enable faster decay of dynamic data

TRB Poly. Lect. 2017

Ans. (c)

236. The disadvantage of write back strategy in cache is that:

(a) it generates repeated memory traffic
(b) it creates a write mechanism whenever there is a write operation to cache
(c) portions of main memory may be invalid
(d) it requires local cache memory attached to every CPU in a multi processor environment

TRB Poly. Lect. 2017

Ans. (c)

237. Which of the following possibilities for saving the return address of a sub- routine, supports sub- routine recursion?

(a) In a processor register
(b) In a memory location associated with the call
(c) On a stack
(d) All of the above

TRB Poly. Lect. 2017

Ans. (c)

238. The unit responsible for tracking the next instruction to be executed in :

(a) ALU
(b) Memory Address Register
(c) Program counter
(d) Instruction memory

TRB Poly. Lect. 2017

Ans. (c)

239. Consider a 32-bit microprocessor having 32-bit instructions, wherein first byte contains the opcode and the remainder the immediate operand or an operand address. How many bits are needed for the program counter and the instruction registers?

(a) 16, 16 (b) 8, 24
(c) 24, 8 (d) 24, 32

UPPCL AE 18.05.2016

Ans. (d) :

240. If a computer's main memory has 2048 locations of each 32 bits, then the total memory capacity is:
(a) 4 KB (b) 8 MB
(c) 4 MB (d) 8 KB
UPPCL AE 18.05.2016

Ans. (d) :

241. The maximum directly addressable memory capacity of a 32- bit microprocessor having 32-bit instructions, wherein first byte contains the opcode and the remainder the immediate operand of an operand address. is:
(a) 16 MB (b) 16KB
(c) 32 MB (d) 16 bytes
UPPCL AE 18.05.2016

Ans. (a) :

242. What is the word- length of the memory, if a CPU has 16 bits address and 1 MB memory access capacity ?
(a) 16 bits (b) 8 bits
(c) 16 bytes (d) 8 bytes
UPPCL AE 18.05.2016

Ans. (c) :

243. Consider a magnetic disc consisting of 200 cylinders, each containing 20 tracks of 10 sectors, and each sector can contain 64 bytes. What is the maximum capacity of the disk?
(a) 2560000 bytes (b) 640 bytes
(c) 12800 bytes (d) 1280000 bytes
UPPCL AE 18.05.2016

Ans. (a) :

244. A memory which has equal access time for all its locations is called:
(a) Read only memory
(b) Sequential access memory
(c) Random access memory
(d) Read- write memory
UPPCL AE 18.05.2016

Ans. (c) :

245. Which of the following assembly codes belongs to general register- based CPU organization?
(a) MULT (b) MULT R1
(c) MULT A (d) MULT R1, R2, R3
UPPCL AE 18.05.2016

Ans. (d) :

246. A pair of base and limit registers in memory defines:
(a) logical address space
(b) network address space
(c) physical address space
(d) mass address space
APPSC Poly. Lect. 13.03.2020

Ans. (a) :

247. A 4-byte data (oX123456AB) is stored in memory with the starting location X. The following options show the possible addresses of the MS and LS bytes in;
i) Little endian and ii) big endian forms. Select the correct option.
(a) i) X = 12, X + 3 = AB; ii) X = 12, X+3 = AB
(b) i) X = AB, X+3 = 12; ii) X = 12, X+3 = AB
(c) i) X = 12, X+3 = AB; ii) X = AB X+3 = 12
(d) i) X = AB, X+3 = 12; ii) X=AB, X+3 = 12
APPSC Poly. Lect. 13.03.2020

Ans. (b) :

248. A computer running windows OS encodes characters in ASCII. What would it produce (ASCII code in hex) at the end of each line in a text file?
(a) 41, 42 (b) OD, OA
(c) 5B, 3F (d) 0A, 32
APPSC Poly. Lect. 13.03.2020

Ans. (b) :

249. You are designing a microprocessor and restricted to have only four bits in the flag register. What are the flags that you should provide in this case considering the most frequently used flags that are needed in a general computing?
(a) Sign, Carry, Parity, Overflow
(b) Parity, Zero, Sign, Overflow
(c) Sign, Zero, Overflow, Carry
(d) Carry, Auxiliary Carry, Parity, Sign
APPSC Poly. Lect. 13.03.2020

Ans. (c) :

250. A translation look aside buffer (TLB), also known as ATC, is a small cache that is a part of memory management hardware that translates:
(a) PNP to NPN (b) NPN to PNP
(c) VPN to PPN (d) PPN to VPN
APPSC Poly. Lect. 13.03.2020

Ans. (c) :

251. A processor has got 16 registers, namely R0 to R15. The instruction format requires 4 bits to express different arithmetic and logic operations. For a three-address instruction, what would be the minimum width (express in number of bits) of an add instruction of the form ADD Rx, Ry, Rz).
(a) 16 (b) 17
(c) 15 (d) 18
APPSC Poly. Lect. 13.03.2020

Ans. (a) :

252. How many bits are used to store the significance in IEEE754 floating point format?
(a) 20 (b) 22
(c) 23 (d) 24
APPSC Poly. Lect. 13.03.2020

Ans. (c) :

253. An 8KB direct- mapped write- back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of the following.
1 Valid bit
1 Modified bit

As many bits as the minimum needed to identify the memory block mapped in the cache.
What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?
(a) 4864 bits (b) 6144 bits
(c) 6656 bits (d) 5376 bits
GATE 2011

Ans. (d) :

254. What type of problem can be caused by the electromagnetic field of speakers?
(a) Distortion of video display
(b) RAM errors
(c) Computer shut down
(d) Read/write problem on magnetic disks and types
UPSC Senior Scientific Officer Grade-II 16.07.2017

Ans. (d) :

255. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in an 4 × 6 array, where each chip is 8k × 4 bits?
(a) 14 (b) 15
(c) 16 (d) 17
UPSC Senior Scientific Officer Grade-II 16.07.2017

Ans. (d) :

256. A 3 bit R/2R, DAC has a reference of 5V. If the values of R and the binary input are 15 k□ and 110 V respectively what is the output voltage?
(a) 0.375 V (b) 3.75 V
(c) 4.25 V (d) 4.28 V
UPSC Senior Scientific Officer Grade-II 16.07.2017

Ans. (b) :

257. The cache memory of 1k words uses direct mapping with a block size of 4 words. How many blocks can be cache accommodate?
(a) 128 words (b) 256 words
(c) 512 words (d) 1024 words
UPSC Senior Scientific Officer Grade-II 16.07.2017

Ans. (b) :

258. For a 32 bit processer with a 32 bit instruction format in which the first 10 bits contains the opcode and the remaining bits contain an operand address. What is the maximum directly addressable memory space?
(a) 16 MB (b) 4 GB
(c) 1 KB (d) 4 MB
UPSC Senior Scientific Officer Grade-II 16.07.2017

Ans. (a) :

259. What is the function performed by the G = A + B + 1 in the ALU operations
(a) Add A, B and increment
(b) Add with Increment B
(c) Addition
(d) Add with carry input of 1
UPPCL AE 2014

Ans. (d) :

260. In the instruction given below which type of Data hazards occur
MULTD R0, R2, R4 and DIVD R10, R0, R6
(a) RAR (b) WAR
(c) RAW (d) WAW
UPPCL AE 2014

Ans. (c) :

261. If n = 10 then total memory locations is
(a) 1 KB (b) 1 MB
(c) 512 B (d) 10 KB
UPPCL AE 2014

Ans. (a) :

262. A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from the main memory. The main memory size is 32 × 128 K.
What is the word length of cache memory
(a) 39 bits (b) 14 bits
(c) 69 bits (d) 78 bits
UPPCL AE 2014

Ans. (d) :

263. When used with an IC, what does the term "QUAD" indicate?
(a) 4 Circuits (b) 6 Circuits
(c) 8 Circuits (d) 2 Circuits
UPPCL AE 2014

Ans. (a) :

264. The memory hierarchy has a hit rate of 80 percent and memory request takes 10ns to complete and memory miss takes 100ns to complete. What is the average access time of the level
(a) 28s (b) 28ns
(c) 28ms (d) 280ns
UPPCL AE 2014

Ans. (b) :

265. Design a hard disk with 32 GB capacity. The hard disk should have 1024 byte sectors, 2048 sectors/track and 4096 tracks/platter. How many platters are required?
(a) 6 (b) 4
(c) 5 (d) 3
UPPCL AE 2014

Ans. (b) :

266. Which system is not true when Multiprocessor systems are classified according to the manner in which CPUs and memory units are associated with one another
(a) NUMA (b) NORMA
(c) UMA (d) NOMA
UPPCL AE 2014

Ans. (d) :

267. A computer consists of a processor and I/O device connected to main memory M via a shared bus with a data bus width of one word. The processor can execute maximum 106 instructions per second. An average instruction requires five machine cycles, three of which use the memory bus. A memory read or write operation uses one machine cycle. Suppose that the processor is continuously executing program that require 95% of its instruction execution rate but not any I/O instructions. Assume that one processor cycle equals one bus cycle. Now suppose the I/O device is to be used to transfer large blocks data between M and D. If programmed I/O is used and each one word I/O transfer requires the processor to execute two instructions estimate the maximum I/O data transfer rate, in words per second, possible through D

(a) 1000000 words/second
(b) 25000 words/second
(c) 50000 words/second
(d) 20000 words/second

UPPCL AE 2014

Ans. (b) :

268. The addressing mode in which no memory reference other than instruction fetch is required to obtain the operand

(a) Direct address
(b) Register address
(c) Immediate address
(d) Register Indirect address

UPPCL AE 2014

Ans. (a) :

269. Which of the following is not the phase of compiler's code generation?

(a) Instruction scheduling
(b) Instruction decoding
(c) Instruction selection
(d) Register allocation

UPPCL AE 2014

Ans. (b) :

270. What is the size of decoder to select row of the chip with size 128×8 RAM, each to address 2048 byte of memory?

(a) 4×16 (b) 4×12
(c) 6×12 (d) 8×16

RPSC ACF & FRO 23.02.2021 (CS)

Ans. (a) :

271. A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : an indirect bit, an opcode a register code part to specify one of 64 registers, and an address part. What is the size of opcode in number of bits?

(a) 6 (b) 7
(c) 8 (d) 9

RPSC ACF & FRO 23.02.2021 (CS)

Ans. (b) :

272. Consider a 4- way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates 20- bit address of a word in main memory. The number of bits in the TAG, LINE and WORD field are respectively.

(a) 9, 6, 5 (b) 7, 7, 6
(c) 7, 5, 8 (d) 9, 5, 6

RPSC ACF & FRO 23.02.2021 (CS)

Ans. (d) :

273. Which of the following is advantage of virtual memory?

(a) Faster access to memory on an average.
(b) Processes can be given protected address spaces.
(c) Linker can assign addresses independent of where the program will be loaded in physical memory
(d) Programs larger than the physical memory size can be run

RPSC ACF & FRO 23.02.2021 (CS)

Ans. (d) :

274. ..... register keeps tracks of the instructions stored in program stored in memory.

(a) AR (Address Register)
(b) XR (Index Register)
(c) PC (Program Counter)
(d) AC (Accumulator)

Punjab PSC Lect. 2016 (IT)

Ans. (c) :

275. 'Aging registers' are.....

(a) Counters which indicate how long ago their associated pages have been referenced
(b) Registers which keep track of when the program last accessed
(c) Counters to keep track of last accessed instruction
(d) Counters to keep track of the latest data structures referred

Punjab PSC Lect. 2016 (IT)

Ans. (a) :

276. Generally Dynamic Ram is used main memory in a computer system as it.....

(a) Consumer less power
(b) has higher speed
(c) has lower cell density
(d) needs refreshing circuitry

Punjab PSC Lect. 2016 (IT)

Ans. (b) :

277. Cache memory works on this principle of.....

(a) Locality of data
(b) Locality of memory
(c) Locality of reference
(d) Locality of reference & memory

Punjab PSC Lect. 2016 (IT)

Ans. (c) :

278. For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, the result is:
(a) the same as if the carry-in is tied LOW since the least significant carry-in is ignored
(b) that carry-out will always be HIGH
(c) a one will be added to the final result
(d) the carry-out is ignored

Punjab PSC Lect. 2016 (IT)

Ans. (c) :

279. What about recursion is true in comparison with iteration?
(a) very expensive in terms of memory
(b) low performance
(c) every recursive program can be written with iteration too.
(d) All of the above

Punjab PSC Lect. 2016 (IT)

Ans. (d) :

280. A front-end processor is:
(a) a user computer system
(b) a processor in a large-scale computer that executes operating system instructions
(c) a minicomputer that relieves main-frame computers at a computer centre of communications control functions
(d) None of the options

Punjab PSC Network Engineer 21.06.2014

Ans. (c) :

281. You wish to install a hardware device that is not Plug and Play. Which of the following is commonly the first instruction given to install this device ?
(a) Install the driver (b) Install the device
(c) Turn the power off (d) Discount the monitor

Punjab State Civil Supplies Corp. Ltd. 13.11.2011

Ans. (c) :

282. Select the statement which is not true in case of a pointer.
(a) Can manipulate data which is at different memory location.
(b) Helps in dynamic memory allocation.
(c) Helps in more compact and efficient coding.
(d) A pointer requires same memory space as the data type which it is pointing to.

Karnataka PSC Comp. Sci. Teacher 16.10.2017

Ans. (d) :

283. In X=(M+N xO)/(P × Q), how many one-address instructions are required to evaluate it?
(a) 4 (b) 6
(c) 8 (d) 10

ISRO Scientist/Engineer 2015

Ans. (c)

284. The minimum time delay between the initiation of two independent memory operations is called
(a) Access time (b) Cycle time
(c) Rotational time (d) Latency time

ISRO Scientist/Engineer 2015

Ans. (b)

285. Increasing the RAM of a computer typically improves performance because
(a) Virtual memory increases
(b) Larger RAMs are faster
(c) Fewer page faults occur
(d) Fewer segmentation faults occur

ISRO Scientist/Engineer 2015

Ans. (c)

286. If there are 32 segments, each size 1 k bytes, then the logical address should have
(a) 13 bits (b) 14 bits
(c) 15 bits (d) 16 bits

ISRO Scientist/Engineer 2015

Ans. (c)

287. How may 32 K ×1 RAM chips are needed to provide a memory capacity of 256 K- bytes?
(a) 8 (b) 32
(c) 64 (d) 128

ISRO Scientist/Engineer 2015

Ans. (c)

288. Which of the given number has its IEEE-754 32-bit floating- point representation as (0 10000000 110 0000 0000 0000 0000 0000)
(a) 2.5 (b) 3.0
(c) 3.5 (d) 4.5

ISRO Scientist/Engineer 2015

Ans. (c)

289. Which of the following is not a valid multicast MAC address?
(a) 01:00:5E:00:00:00
(b) 01:00:5E:00:00: FF
(c) 01:00:5E:00: FF: FF
(d) 01:00:5E:FF: FF: FF

ISRO Scientist/Engineer 2014

Ans. (d)

290. How much memory is required to implement z-buffer algorithm for a 512×512×24 bit-plane image
(a) 768 KB (b) 1 MB
(c) 1.5 MB (d) 2MB

ISRO Scientist/Engineer 2014

Ans. (c)

291. Suppose you want to build a memory with 4 byte word and a capacity of 2^{21} bits. What is type of decoder required if the memory is built using 2K× 8 RAM chips?
(a) 5 to 32 (b) 6 to 64
(c) 4 to 16 (d) 7 to 128

ISRO Scientist/Engineer 2014

Ans. (a)

292. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4×6 array, where each chip is 8K×4 bits?
(a) 13 (b) 15
(c) 16 (d) 17

ISRO Scientist/Engineer 2014

Ans. (d)

293. The number of logical CPUs in a computer having two physical quad-core chips with hyper threading enabled is_____.
(a) 1 (b) 2
(c) 8 (d) 16
ISRO Scientist/Engineer 2014

Ans. (d)

294. Consider a 33 MHz CPU based system. What is the number of wait states required if it is interfaced with a 60ns memory? Assume a maximum of 10ns delay for additional circuitry like buffering and decoding.
(a) 0 (b) 1
(c) 2 (d) 3
ISRO Scientist/Engineer 2014

Ans. (c)

295. Consider a small 2-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8,12,0,12,8
(a) 2 (b) 3
(c) 4 (d) 5
ISRO Scientist/Engineer 2007

Ans. (c)

296. In comparison with static RAM memory, the dynamic RAM memory has
(a) lower bit density and higher power consumption
(b) higher bit density and higher power consumption
(c) lower bit density and lower power consumption
(d) higher bit density and lower power consumption
ISRO Scientist/Engineer 2007

Ans. (b)

297. Virtual memory is
(a) Part of Main Memory only used for swapping
(b) A technique to allow a program, of size more than the size of the main memory, to run
(c) Part of secondary storage used in program execution
(d) None of these
ISRO Scientist/Engineer 2007

Ans. (b)

298. The principal of locality of reference justifies the use of
(a) virtual memory (b) interrupts
(c) main memory (d) cache memory
ISRO Scientist/Engineer 2007

Ans. (d)

299. For converting a virtual address into the physical address, the programs are divided into _____
(a) Pages (b) Frames
(c) Segments (d) Blocks
GPSC Asstt. Prof. 30.06.2016

Ans. (a) :

300. The cache bridges the speed gap between _____ and _____
(a) RAM and ROM
(b) RAM and Secondary memory
(c) Processor and RAM
(d) None of the above
GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

301. When the processor receives the request from a device, it responds by sending _____
(a) Acknowledge signal (b) BUS grant signal
(c) Response signal (d) None of the above
GPSC Asstt. Prof. 30.06.2016

Ans. (b) :

302. The disadvantage of DRAM over SRAM is/are _____
(a) Lower data storage capacities
(b) Higher heat dissipation
(c) The cells are not static
(d) All of the above
GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

303. The block transfer capability of the DRAM is called _____
(a) Burst mode (b) Block mode
(c) Fast page mode (d) Fast frame mode
GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

304. The iconic feature of the RISC machine among the following is _____
(a) Reduced number of addressing modes
(b) Increased memory size
(c) Having a branch delay slot
(d) All of the above
GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

305. Out of the following which is not a CISC machine.
(a) IBM 370/168 (b) VAX 11/780
(c) Intel 80486 (d) Motorola A567
GPSC Asstt. Prof. 30.06.2016

Ans. (d) :

306. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy ____ bits.
(a) 24 (b) 23
(c) 20 (d) 16
GPSC Asstt. Prof. 30.06.2016

Ans. (b) :

307. The main advantage of multiple bus organization over a single bus is _____
(a) Reduction in the number of cycles for execution
(b) Increase in size of the registers
(c) Better Connectivity
(d) None of the above
GPSC Asstt. Prof. 30.06.2016

Ans. (a) :

308. The return address from the interrupt-service routine is stored on the _____

(a) System heap (b) Processor register
(c) Processor stack (d) Memory

GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

309. The time between the receiver of an interrupt and its service is _____

(a) Interrupt delay (b) Interrupt latency
(c) Cycle time (d) Switching time

GPSC Asstt. Prof. 30.06.2016

Ans. (b) :

310. The write-through procedure is used _____

(a) To write onto the memory directly
(b) To write and read from memory simultaneously
(c) Both (a) and (b)
(d) None of the above

GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

311. A message is authenticated using _____ in SSL.

(a) MAC (Message Access Code)
(b) MAC (Message Authentication Code)
(c) MAC (Machine Authentication Code)
(d) MAC (Machine Access Code)

GPSC Asstt. Manager 13.12.2020 (IT)

Ans. (b) :

312. S/MIME is an acronym for

(a) Secure/Multimedia Internet Mailing Extensions
(b) Secure/Multipurpose Internet Mailing Extensions
(c) Secure/Multimedia Internet Mail Extensions
(d) Secure/Multipurpose Internet Mail Extensions

GPSC Asstt. Manager 13.12.2020 (IT)

Ans. (d) :

313. The command used to get the size of hdisk0 in an AIX LPAR set of virtual disks is

(a) Isdev (b) Iquervpv
(c) Isattr (d) Getconf

GPSC Asstt. Manager 13.12.2020 (IT)

Ans. (d) :

314. Which of the following is non- emissive display devices?

(a) CRT display
(b) Plasma panel display
(c) LCD
(d) LED
(e) Electroluminescent display

CGPSC Asstt. Prof. 2014 (CS)

Ans. (c)

315. In a two- pass assembler, which of the following is not a valid task of pass-1?

(a) To determine the length of machine instruction
(b) To keep track of location counter
(c) To generate symbol table
(d) To generate literal table
(e) To process pseudo ops

CGPSC Asstt. Prof. 2014 (CS)

Ans. (e)

316. Which of the following is not a valid operating system functionality in connection with file management?

(a) Creating and deleting file
(b) Creating and deleting directories
(c) Storage allocation
(d) Mapping files onto secondary storage
(e) Backing up files on stable storage media

CGPSC Asstt. Prof. 2014 (CS)

Ans. (c)

317. Which of the following is an unguided transmission media?

(a) Magnetic media
(b) Twisted pair
(c) Radio transmission
(d) Coaxial cable
(e) Fiber optics

CGPSC Asstt. Prof. 2014 (CS)

Ans. (c)

318. The number of lines contained in a set associative cache can be calculated from

(a) the number of bits in the memory address, the number of bits assigned to the tag and the number of bits assigned to the set id
(b) the number of bits in the memory address, the number of bits assigned to the tag, the number of bits assigned to the set id and the number of bits assigned to the word id (identifying the number of words per block)
(c) the number of bits in the memory address, the number of bits assigned to the set id and the number of bits assigned to the word id (indentifying the number of word per block)
(d) None of the above

BPSC Asstt. Prof. 21.09.2021

Ans. (b) :

319. The principle of locality of reference justifies the use of

(a) virtual memory (b) interrupts
(c) cache memory (d) secondary memory

APPSC Lect. Degree College 07.06.2017 (CS)

Ans. (c) :

320. How many 8-bit characters can be transmitted per second over a 9600 baud serial communication link using asynchronous mode of transmission with one start bit, eight data bits, two stop bits, and one parity bit?

(a) 600 (b) 800
(c) 876 (d) 1200

APPSC Lect. Degree College 07.06.2017 (CS)

Ans. (b) :

321. The Mapping of IP address to MAC address is done by

(a) ARP (b) RARP
(c) DHCP (d) RSVP

TANGEDCO AE 2018

Ans. (a)

322. Address bits needed to select all locations in memory if 16K×8 RAM

(a) 8 bits (b) 10 bits
(c) 14 bits (d) 16 bits

TANGEDCO AE 2018

Ans. (c)

323. The ALU makes use of _____to store the intermediate results.

(a) Accumulator (b) Registers
(c) Heap (d) Stack

TANGEDCO AE 2018

Ans. (a)

324. The vector architecture of processor belongs to the Flynn's taxonomy of

(a) SISD (b) SIMD
(c) MIMD (d) MISD

TANGEDCO AE 2018

Ans. (b)

325. What happens, when a program tries to access a page that is mapped in address space but not loaded in physical memory?

(a) Segmentation fault occurs
(b) Fatal error occurs
(c) Page fault occurs
(d) No error occurs
(e) System error occurs

CGPSC Asstt. Prof. 2014 (IT)

Ans. (c) :

326. A file of size 2000KB is to be sent from station A to station B through a link. The RTT is 200ms and size of packet is 1KB. Link bandwidth is infinite which implies that the transmit time of a packet is nearby zero. Initially 3xRTT time is takes for 'handshaking' before data is sent. Packets are sent in a special way, like one packet is sent during the first RTT, two packets are sent during the second RTT, four packets are sent during the third RTT and so on. What will be the total time required to transfer the file?

(a) 2.4s (b) 2.5s
(c) 2.6s (d) 2.7s

RPSC VPIITI 2012 (CS)

Ans. (d) :

327. Consider the following statements: I. A logical address does not refer to an actual existing address in memory II. A physical address that refers to an actual physical address in memory. Which of the following is correct ?

(a) I
(b) II
(c) Both the correct
(d) None of the statement are correct

RPSC VPIITI 2012 (CS)

Ans. (c) :

328. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20 - bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively :-

(a) 9, 6, 5 (b) 7, 7, 6
(c) 7, 5, 8 (d) 9, 5, 6

RPSC VPIITI 2012 (CS)

Ans. (b) :

329. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively :

(a) 256 Mbyte, 19 bits (b) 256 Mbyte, 28 bits
(c) 512 Mbyte, 20 bits (d) 64 Gbyte, 28 bit

RPSC VPIITI 2012 (CS)

Ans. (a) :

330. A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcomes is known. A program executes 10^8 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is :

(a) 1.0 second (b) 1.2 seconds
(c) 1.4 seconds (d) 1.6 seconds

RPSC VPIITI 2012 (CS)

Ans. (b) :

331. Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line ?

(a) Neither vectored interrupt nor multiple interrupting devices are possible
(b) Vectored interrupts are not possible but multiple interrupting devices are possible.
(c) Vectored interrupts and multiple interrupting devices are both possible
(d) Vectored interrupt is possible but multiple interrupting devices are not possible

RPSC VPIITI 2012 (CS)

Ans. (b) :

332. The instruction, Add # 45, R1 does :

(a) Adds the value of 45 to the address of R1 and stores 45 in that address
(b) Adds 45 to the value of R1 and stores in R1
(c) Finds the memory location 45 and adds that content to that of R1
(d) None of these

RPSC VPIITI 2012 (CS)

Ans. (b) :

333. A set associative cache consists of 64 lines, or slots divided into four lines sets. Main memory consists of 4k blocks of 128 words each. What are the number of the bits of TAG. Set offset and word offset respectively ?

(a) 8, 4, 7 (b) 7, 5, 7
(c) 7, 5, 8 (d) 8, 5, 6

RPSC VPIITI 2012 (CS)

Ans. (a) :

334. What is the source and destination addressing mode for the instruction ?

ADD Ax, [500];
Ax ← M[500];

(a) Immediate memory direct
(b) Memory direct & Register indirect
(c) Memory direct & Register direct
(d) Memory indirect & Register indirect

RPSC VPIITI 2012 (CS)

Ans. (c) :

335. Consider a cache with 40 bit address 16384 blocks and block size is 256 byte Tags are 19 bit long. How many sets are there and what is the associating of a cache ?

(a) 1024 sets, 8 way set associative
(b) 4096 sets, 4 way set associative
(c) 8192 sets, 2 way set associative time
(d) None of these

RPSC VPIITI 2012 (CS)

Ans. (c) :

336. What is the address of the operand in a computation- type instruction :-

(a) Direct Address (b) Relative Address
(c) Effective Address (d) Register Address

RPSC VPIITI 2012 (CS)

Ans. (c) :

337. A certain processor uses a fully associative cache of size 16 kB. The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the Tag and the Index fields respectively in the address generated by the processor?

(a) 24 bits and 0 bits (b) 28 bits and 4 bits
(c) 24 bits and 4 bits (d) 28 bits and 0 bits

GATE-2019

Ans. (d) :

338. The total time to prepare a disk drive mechanism for a block of data to be read from it is

(a) seek time
(b) latency
(c) latency plus seek time
(d) transmission time

ISRO Scientist/Engineer 2008

Ans. (c)

339. The device which is used to connect a peripheral to bus is known as

(a) control register
(b) interface
(c) communication protocol
(d) none of these

ISRO Scientist/Engineer 2008

Ans. (b)

340. Which of the following architecture is/are not suitable for realising SIMD?

(a) Vector processor (b) Array processor
(c) Von Neumann (d) All of the above

ISRO Scientist/Engineer 2008

Ans. (c)

341. More than one word are put in one cache block to

(a) exploit the temporal locality of reference in a program
(b) exploit the spatial locality of reference in a program
(c) reduce the miss penalty
(d) none of these

ISRO Scientist/Engineer 2008

Ans. (b)

342. The performance of a pipelined processor suffers if

(a) The pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of these

ISRO Scientist/Engineer 2008

Ans. (d)

343. A computer which issues instructions in order, has only 2 registers and 3 opcodes ADD, SUB and MOV. Consider 2 different implementations of the following basic block:

Case 1	Case2
t1 = a + b;	t2 = c + d;
t2 = c + d;	t3 = e – t2;
t3 = e + t2;	t1 = a + b;
t4 = t1 + t2;	t4 = t1 – t2;

Assume that all operands are initially in memory. Final value of computation also has to reside in memory. Which one is better in terms of memory accesses and by how many MOV instructions?

(a) Case 2, 2 (b) Case 2, 3
(c) Case 1, 2 (d) Case 1, 3

ISRO Scientist/Engineer 2020

Ans. (*)

344. Which of the following is a type of a out–of–order execution, with the reordering done by a compiler.

(a) Loop unrolling
(b) Dead code elimination
(c) Strength reduction
(d) Software pipelining

ISRO Scientist/Engineer 2020

Ans. (d)

345. A non–pipelined CPU has 12 general purpose registers (R0, R1, R1, …..R12). Following operations are supported
ADD Ra, Rb, Rr Add Ra to Rb and store the result in Rr
MUL Ra, Rb, Rr Multiply Ra to Rb and store the result in Rr
MUL operations takes two clock cycles, ADD takes one clock cycle.
Calculate minimum number of clock cycles required to compute the value of the expression XY + XYZ + YZ. The variables X, Y, Z are initially available in registers R0, R1 and R2 and contents of these registers must not be modified.
(a) 5 (b) 6
(c) 7 (d) 8
ISRO Scientist/Engineer 2020

Ans. (b)

346. One instruction tries to write an operand before it is written by previous instruction. This may lead to a dependency called
(a) True dependency
(b) Anti–dependency
(c) Output dependency
(d) Control hazard
ISRO Scientist/Engineer 2020

Ans. (c)

347. Remote Procedure Calls are used for
(a) communication between two processes remotely different from each other on the same system
(b) Communication between two processes on the same system
(c) Communication between two processes on separate systems
(d) None of the above
ISRO Scientist/Engineer 2020

Ans. (*)

348. A magnetic disk has 100 cylinders, each with 10 tracks of 10 sectors. If each sector contains 128 bytes, what is the maximum capacity of the disk in kilobytes?
(a) 1,280,000 (b) 1280
(c) 1250 (d) 128,000
ISRO Scientist/Engineer 2020

Ans. (b)

349. How many total bits are required for a direct-mapped cache with 128 KB of data and 1 word block size, assuming a 32 bit address and 1 word size of 4 bytes?
(a) 2 Mbits (b) 1.7 Mbits
(c) 2.5 Mbits (d) 1.5 Mbits
ISRO Scientist/Engineer 2020

Ans. (d)

350. which of the following is an efficient method of cache updating?
(a) Snoopy writes (b) Write through
(c) Write within (d) Buffered write
ISRO Scientist/Engineer 2020

Ans. (a)

351. The immediate addressing mode can be used for
1. Loading internal registers with initial values
2. Perform arithmetic or logical operation on data contained in instructions.
Which of the following is true?
(a) Only 1
(b) Only 2
(c) Both 1 and 2
(d) Immediate mode refers to data in cache
ISRO Scientist/Engineer 2020

Ans. (c)

352. Statements associated with registers of CPU are given. Identify the false statement.
(a) The program counter holds the memory address of the instruction in execution.
(b) Only opcode is transferred to the control unit.
(c) an instruction in the instruction register consists of the opcode and the operand
(d) The value of the program counter is incremented by 1 once its value has been read to the memory address register.
ISRO Scientist/Engineer 2020

Ans. (a)

353. Which of the following affects the processing power assuming they do not influence each other.
(1) Data bus capability
(2) Addressing scheme
(3) Clock speed
(a) 3 only (b) 1 and 3 only
(c) 2 and 3 only (d) 1, 2 and 3
ISRO Scientist/Engineer 2020

Ans. (d)

354. Consider a 32-bit processor which supports 70 instructions. Each instruction is 32 bit long and has 4 fields namely opcode, two register identifiers and an immediate operand of unsigned integer type. Maximum value of the immediate operand that can be supported by the processor is 8191. How many registers the processor has?
(a) 32 (b) 64
(c) 128 (d) 16
ISRO Scientist/Engineer 2020

Ans. (b)

355. In which parallel computer, the same instruction is executed synchronously by all processing units?
(a) SISD (b) SIMD
(c) MISD (d) MIMD
UPSC Poly Lect. 10.03.2019

Ans. (b) :

356. The ratio of time taken by single processor system and that taken by a parallel processing system is called:
(a) Efficiency (b) Speed up
(c) Throughput (d) Turnaround time
UPSC Poly Lect. 10.03.2019

Ans. (b) :

357. The hardware technique that detects and resolves hazards is called:
(a) Interlock (b) Intralock
(c) Halt (d) Inter unlock
UPSC Poly Lect. 10.03.2019

Ans. (a) :

358. If the time to transfer a block from the controller to memory over the bus is longer than the time to read a block from the disk, it may be necessary to read one block and then skip two or more blocks is called:
(a) Spooling (b) Interleaving
(c) Interlinking (d) Data hiding
UPSC Poly Lect. 10.03.2019

Ans. (b) :

359. A general solution for the machine with many completely independent address spaces which can grow or shrink independently, without affecting each other?
(a) Paging (b) Segmentation
(c) Framing (d) Spooling
UPSC Poly Lect. 10.03.2019

Ans. (b) :

360. For a bus frequency of 100 MHz and with data being transferred at 64 bits at a time. The DDR SDRAM gives a transfer rate of:
(a) 800 MB/S (b) 1600 MB/S
(c) 3200 MB/S (d) 6400 MB/S
UPSC Poly Lect. 10.03.2019

Ans. (b) :

361. A block set-associative cache consists of a total of 64 blocks divided into four-block sets. The main memory contains 4096 blocks, each consisting of 128 words. The number of bits in main memory address will be:
(a) 17 bits (b) 18 bits
(c) 19 bits (d) 20 bits
UPSC Poly Lect. 10.03.2019

Ans. (c) :

362. What would be the speed of a processor in terms instructions per second if the processor has two types of instructions A and B. Type A instructions take 18 clock cycles and type B instructions take 8 clock cycles, Programs on an average use 20% of type A and 80% of type B instructions. The clock rate is of 1 GHz.
(a) 1000MIPS (b) 10MIPS
(c) 100MIPS (d) 10000MIPS
TSPSC Manager 2015

Ans. (c) :

363. Booth's algorithm is used to____ signed number (2's complement)
(a) add (b) subtract
(c) multiply (d) divide
TSPSC Manager 2015

Ans. (c) :

364. An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as
(a) DMA (b) UART
(c) USRT (d) Serial Interface
TSPSC Manager 2015

Ans. (a) :

365. In a 32- bit floating- point format, the leftmost bit stores the sign of the number. The exponent value is stored in the next eight bits. A bias of 127 is subtracted from the field to get the true exponent value. The base is assumed to be 2. The format stores a normalized floating- point number, with the left- most being implicit. Thus remaining 23 bits are used to store 24-bit significant. What is the highest positive integer that can be represented
(a) 2^{128} (b) $(2-2^{-23}) \times 2^{128}$
(c) 2^{127} (d) $(2-2^{-23}) \times 2^{127}$
TSPSC Manager 2015

Ans. (b) :

366. The instruction of a micro programmed control unit is called as
(a) micro- instruction
(b) micro- operation
(c) machine instruction
(d) micro- program
TSPSC Manager 2015

Ans. (a) :

367. Suppose that a bus has 16 data lines and requires 4 cycles of 250nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?
(a) 1 Megabyte/sec (b) 4 Megabytes/sec
(c) 8 Megabytes/sec (d) 2 Megabytes/sec
TSPSC Manager 2015

Ans. (d) :

368. Which of the following activities is not done by memory management?
(a) Keep an account of which part of memory are currently being used by each of the processes
(b) Decide which processes are to be brought into memory when memory space becomes available
(c) Allocate and de- allocate memory space as needed
(d) Storage allocation
TSPSC Manager 2015

Ans. (d) :

369. Which of the following techniques can be used to counter the problem of external fragmentation that occurs in dynamic partitioning memory management?
(a) Compaction (b) Segmentation
(c) Swapping (d) Splitting
TSPSC Manager 2015

Ans. (a) :

370. A 32 bit adder is formed by cascading 4 bit CLA adder. The gate delays (latency) for getting the sum bits is

(a) 16 (b) 18
(c) 17 (d) 19

ISRO Scientist/Engineer 17.12.2017

Ans. (b) :

371. We consider the addition of two 2's compliment number $b_{n-1}b_{n-2}\ldots b_0$ and $a_{n-1}a_{n-2}\ldots a_0$. A binary adder for adding two unsigned binary number is used to add two binary number. The sum is denoted by $c_{n-1}C_{n-2}\ldots c_0$ The carry out is denoted by c_{out}. The overflow condition is identified by

(a) $c_{out}\left(\overline{a_{n-1}Åb_{n-1}}\right)$

(b) $\overline{a_{n-1}}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}b_{n-1}}c_{n-1}$

(c) $c_{out} \oplus c_{n-1}$

(d) $a_{n-1} \oplus b_{n-1} \oplus C_{n-1}$

ISRO Scientist/Engineer 17.12.2017

Ans. (c) :

372. Station A uses 32 byte packets to transmit messages to Station B using a sliding window protocol. The round trip time delay between A and B is 40 ms and the bottleneck bandwidth on the path A and B is 64 kbps. What is the optimal window size that A should use?

(a) 5 (b) 10
(c) 40 (d) 80

ISRO Scientist/Engineer 17.12.2017

Ans. (b) :

373. A two way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The physical address space is 4 GB. The number of bits in the TAG, SET fields are

(a) 20, 7 (b) 19, 8
(c) 20, 8 (d) 21, 9

ISRO Scientist/Engineer 17.12.2017

Ans. (b) :

374. A CPU has a 32 KB direct mapped cache with 128 byte block size. Suppose A is a 2 dimensional array of size 512 × 512with elements that occupy 8 bytes each. Consider the code segment

```
for (i = 0; i< 512; i++){
  for (j = 0; j < 512; j++){
        x+=A [i][j];
  }
}
```

Assuming that array is stored in order A [0][0], A[0][1], A[0][2]……. the number of cache misses is

(a) 16384 (b) 512
(c) 2048 (d) 1024

ISRO Scientist/Engineer 17.12.2017

Ans. (a) :

375. A computer with 32 bit word size uses 2s compliment to represent to represent numbers. The range of integers that can be represented by this computer is

(a) -2^{32} to 2^{32} (b) -2^{31} to $2^{32}-1$
(c) -2^{31} to $2^{32}-1$ (d) $-2^{31}-1$ to $2^{32}-1$

ISRO Scientist/Engineer 17.12.2017

Ans. (c) :

376. Let M = 11111010 and N = 00001010 be two 8 bit two's compliment number. Their product in two's complement is

(a) 11000100 (b) 10011100
(c) 10100101 (d) 11010101

ISRO Scientist/Engineer 17.12.2017

Ans. (a) :

377. For a pipelines CPU with a single ALU, consider the following:

A. The j + 1st instructions uses the result of jth instruction as an operand
B. conditional jump instruction
C. jth and j + 1st instructions require ALU at the same time

Which one of the above causes a hazard?

(a) A and B only (b) B and C only
(c) B only (d) A, B, C

ISRO Scientist/Engineer 17.12.2017

Ans. (d) :

378. In designing a computer's cache system, the cache block for cache line) size is an important parameter. Which one of the following statements is correct in this context?

(a) Smaller block size incurs lower cache miss penalty
(b) Smaller block size implies better spatial locality
(c) Smaller block size implies smaller cache tag
(d) Smaller block size implies lower cache hit time

ISRO Scientist/Engineer 17.12.2017

Ans. (a) :

379. Consider an instruction of the type LW R1, 20(R2) which during execution reads a 32 bit word from memory and stores it in a 32 bit register R1. The effective address of the memory location is obtained by adding a constant 20 and contents of R2. Which one best reflects the source operand

(a) Immediate addressing
(b) Register addressing
(c) Register indirect addressing
(d) Indexed addressing

ISRO Scientist/Engineer 17.12.2017

Ans. (c) :

380. Consider a 4-dimensional dataset with attributes A,B,C,D described in terms of 10,4,50,20 distinct values respectively. Assuming that each cell occupied 2 bytes of memory, what is the total memory space required to materialize all possible 3-Dimensional cuboids of the dataset?

(a) 32,000 bytes (b) 33,600 bytes
(c) 16,800 bytes (d) 14,800 bytes

APPSC Lect. 2017 (Degree College) (CS)

Ans. (b) :

381. Triple Modular Redundancy (TMR) for fault tolerance is characterized by

(a) Each device is replicated three times
(b) Each voter is a circuit that has three inputs and one output
(c) Each device is replicated three times and Each voter is a circuit that has three inputs one output
(d) None of the given options

APPSC Lect. 2017 (Degree College) (CS)

Ans. (a) :

382. which of the following is NOT a method used for data transfer between peripherals and memory?

(a) Programmed I/O
(b) Interrupt initiated I/O
(c) Direct Memory Access
(d) Pipelining

APPSC Lect. 2017 (Degree College) (CS)

Ans. (d) :

383. How many 64K×1RAM chips are required to provide a memory of size 256K bytes?

(a) 8 (b) 4
(c) 32 (d) 64

APPSC Lect. 2017 (Degree College) (CS)

Ans. (c) :

384. Consider a hard disk containing 1000 cylinders, 10 platters each with 2 recording surfaces and 63 sectors per track. What is the position of the sector whose 3-D disk address is 200,15,55> representing cylinder, surface, sector numbers respectively.

(a) 3520 (b) 253000
(c) 50600 (d) 250600

APPSC Lect. 2017 (Degree College) (CS)

Ans. (b) :

385. When a cache memory is 30 times faster than main memory/RAM and cache hit ratio is 90%, the speed up gained using the cache is approximately.....

(a) 10 times (b) 7.7 times
(c) 2.7 times (d) 27 times

APPSC Lect. 2017 (Degree College) (CS)

Ans. (b) :

386. How much speed do we gain by using the cache, when cache is used 80% of the time? Assume cache is faster than main memory.

(a) 5.27 (b) 2.00
(c) 4.16 (d) 6.09

ISRO Scientist/Engineer 2013

Ans. (c) :

387. In which of the following modes of I/O data transfer does the peripheral interact directly with the memory?

(a) Programmed I/O (b) Interrupt I/O
(c) Direct memory access (d) Peripheral access

APPSC Lect. Degree College 16.09.2020

Ans. (c) :

388. Given the following table for a program trace experiment:

Instruction type	CPI	Instruction Mix (in %)
Arithmetic and logic	1	55
Load/store with cache hit	2	22
Branch	4	14
Memory reference with cache miss	8	9

Calculate the performance of the processor in terms of MIPS, given that it executes a million instructions on 300-MHz processor.

(a) 178 (b) 132
(c) 194 (d) 185

APPSC Lect. Degree College 16.09.2020

Ans. (b) :

389. Which of the following allows direct data transfer between a device and main memory without involving the processor ?

(a) RAM (b) CPU
(c) DMA (d) PROM

RPSC ACF FRO 23.02.2021 (Comp. App./Sci.)

Ans. (c) :

390. For a multi-processor architecture, in which protocol a write transaction is forwarded to only those processors that are known to possess a copy of newly altered cache line?

(a) Snoopy bus protocol
(b) Cache coherency protocol
(c) Directory based protocol
(d) None of the above

ISRO Scientist/Engineer 22.04.2018

Ans. (c) :

391. Of the following, which best characterizes computers that use memory-mapped I/O?

(a) The computer provides special instructions for manipulating I/O ports
(b) I/O ports are placed at addresses on the bus and are accessed just like other memory locations
(c) To perform I/O operations, it is sufficient to place the data in an address register and call channel in perform the operation
(d) I/O can be performed only when memory management hardware is turned on

ISRO Scientist/Engineer 22.04.2018

Ans. (b) :

392. A byte addressable computer has a memory capacity of 2^mKB (kbytes) and can perform 2^n operations. An instruction involving 3 operands and one operator needs maximum of

(a) 3m bits
(b) 3m + n bits
(c) m + n bits
(d) none of the above

ISRO Scientist/Engineer 22.04.2018

Ans. (d) :

393. The first item defined for a new system is its:

(a) Storage (b) Outputs
(c) Inputs (d) Processing
(e) Design

CGPSC Asstt. Prof. 2014 (Comp. App.)

Ans. (b) :

394. An operation that enables us to define cursor and assign a name to it:

(a) Declaring (b) Stating
(c) Extracting (d) Importing
(e) Exporting

CGPSC Asstt. Prof. 2014 (Comp. App.)

Ans. (a) :

395. On which principle does a Cache memory works?

(a) Locality of data
(b) Locality of memory
(c) Locality of reference
(d) Locality of reference and memory
(e) Locality of control

CGPSC Asstt. Prof. 2014 (Comp. App.)

Ans. (c) :

396. For a memory system having the following specification : size of the main memory is 4 K blocks, size of the cache is 128 blocks and the block size is 16 words. Assuming that the system uses associative mapping, the cache field parameters would be

(a) Word field = 6 bits, Tag field = 10 bits, No. of bits in main memory address = 14
(b) Word field = 4 bits, Tag field = 10 bits, No. of bits in main memory address = 14
(c) Word field = 6 bits, Tag field = 12 bits, No. of bits in main memory address = 16
(d) Word field = 4 bits, Tag field = 12 bits, No. of bits in main memory address = 16

RPSC VPITI 2018 (CS)

Ans. (d) :

397. How many RAM chips are required to construct 256 K × 16 memory using 16 K × 1 RAM ?

(a) 512
(b) 256
(c) 128
(d) 56

RPSC VPITI 2018 (CS)

Ans. (b) :

398. Whenever the two instructions needs the same hardware resource at the same instants of time, the following pipeline hazard occurs :

(a) Data hazard
(b) Structure hazard
(c) Control hazard
(d) Both control and data hazard

RPSC VPITI 2018 (CS)

Ans. (b) :

399. A block of addresses is granted to a small organization. If one of the address is 205.16.37.39/28. What is the value of first address and total number of addresses in the block ?

(a) 205.16.37.34, 14
(b) 205.16.37.32, 16
(c) 205.16.37.36, 12
(d) 205.16.37.38, 8

RPSC VPITI 2018 (CS)

Ans. (b) :

400. The use of which one of the following in a computer is justified by the principle of locality?

(a) DMA
(b) Virtual Memory
(c) Software Interrupt
(d) Cache Memory

RPSC VPITI 2018 (CS)

Ans. (d) :

401. Instruction pipeline cannot deviate from its normal operation due to

(a) resource conflicts
(b) data dependency conflicts
(c) time delay variation in segments
(d) branch difficulties

RPSC VPITI 2018 (CS)

Ans. (c) :

02. DATA STRUCTURES

Elementary Data Organization, Built in Data Types in C/C++/JAVA. Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations : Big Oh, Big Theta and Big Omega, Time-Space trade-off. Abstract Data Types (ADT), Arrays and Application of arrays, parse Matrices and their representations. Linked lists, Stacks, Queues, Searching and sorting Graphs, Tree, Binary Tree and its applications, Hashing, B+ tree.

1. The minimum number of bits required to represent numbers in the range –28 to +31 is
(a) 5 (b) 6
(c) 7 (d) 8
RPSC Lect. 2011

Ans. (b) :

2. Which of the following data types is not supported by C language
(a) char (b) long
(c) double (d) string
RPSC Lect. 2011

Ans. (d) :

3. What shall be output of following statement ?
unsigned char c;
c = c ≫8;
(a) zero if c is even and one if c is odd
(b) one if c is even and zero if c is odd
(c) zero if c $\geq$ 128 otherwise one
(d) zero if c $\leq$ 128 otherwise one
RPSC Lect. 2011

Ans. (*) :

4. Which of the following sorting methods is not suited for an already sequence?
(a) merge sort (b) selection sort
(c) bubble sort (d) insertion sort
RPSC Lect. 2011

Ans. (b) :

5. In a double linked list, next and prev are pointers to next and previous, nodes of the current node. For first node, prev is null and for last node next is null. Following four statements are needed to insert a new node x after node t.
(Statement A) t- >next =x;
(Statement B) x- >prev =t;
(Statement C) x- >next = t->next;
(Statement D) t- >next-> prev = x;
Correct order of these statements for insertion shall be
(a) C, D, A, B (b) A, B, C, D
(c) D, C, B, A (d) B, C, A, B
RPSC Lect. 2011

Ans. (a) :

6. Minimum and maximum height of a binary search tree of n nodes is
(a) 1, $\log_2 n$ (b) $\log_2 n$, $\log_2 n$
(c) $\log_2 n$, n (d) n, n^2
RPSC Lect. 2011

Ans. (c) :

7. Which of the following statements describe Binary Search Tree correctly?
For every node, value
(a) is more than value at its left child and less than value at its right child.
(b) is less than value at both its left and right child.
(c) is more than value at any node in left subtree and less than value at any node in its right subtree
(d) Both (1) and (3)
RPSC Lect. 2011

Ans. (d) :

8. Consider n elements a_1, a_2....., a_{n-1}, a_n. These elements are pushed into stack one by one. After every two push, one pop operation is carried out. Contents of stack after all elements have been pushed shall be
(a) a_1, a_3, a_5,..... a_{n-1} (n is even) otherwise a_1, a_3, a_5..... a_{n-2}, a_n (n is odd)
(b) a_2, a_4, a_6,..... a_n (n is even) otherwise a_2, a_4, a_6..... a_{n-2}, a_{n-1} (n is odd)
(c) a_1, a_3, a_5,..... a_{n-1} (n is even) otherwise a_2, a_4, a_6..... a_{n-2}, a_{n-1} (n is odd)
(d) a_2, a_4, a_6,..... a_n (n is even) otherwise a_1, a_3, a_5..... a_{n-2}, a_n (n is odd)
RPSC Lect. 2011

Ans. (a) :

9. In order and preorder traversal of a tree are UVXQTWRN and QXUVTRWN. Postorder traversal for this tree is given by
(a) VUXTWNRQ (b) VUXWNRTQ
(c) VUXWNTRQ (d) VUXWRNTQ
RPSC Lect. 2011

Ans. (b) :

10. Binary search is applicable in
(a) Array and AVL tree
(b) Array and Heap tree
(c) Queue and AVL tree
(d) Queue and Heap tree
RPSC Lect. 2011

Ans. (a) :

11. Lexicographical ordering refers to occurrence of words in dictionary. As "Above" comes before. "Able", "Above" < "Able" in lexicographical ordering. Time complexity to determine lexicographical ordering of two English words of length m and n is

(a) $O(\log_2(m+n))$ (b) $O(m+n)$
(c) $O(\min(m,n))$ (d) $O(max(m,n))$

RPSC Lect. 2011

Ans. (c) :

12. Pointer head points to first node of a linked list Each node has link to next node. Time complexity to swap values of p^{th} and q^{th} nodes shall be

(a) $O(p^2+q^2)$ (b) O(max (p,q))
(c) O(1) (d) $O((p+q)^2)$

RPSC Lect. 2011

Ans. (b) :

13. Every node of a tree has exactly 3 children. If root is at height 1, number of nodes in a full tree (every level is full except last level that consists of leaf nodes only) of height h is given by

(a) $(3^h-1)/2$ (b) $(3^{h+1}-1)/2$
(c) $(3^{h-1}-1)/2$ (d) (3^h-1)

RPSC Lect. 2011

Ans. (a) :

14. The best data structure to check whether an arithmetic expression has balanced parentheses is a/an

(a) stack (b) priority queue
(c) array (d) linked list

RPSC Lect. 2011

Ans. (a) :

15. In a 12 bit integer, least significant bit is set to zero and most significant bit is set to one. Range of values this integer can assume is

(a) {0, 2, 4, 8,……..2048}
(b) {2048,2050,……..4094}
(c) {0, 1, 2, 3,……..2048}
(d) {2048,2049,…….4095}

RPSC Lect. 2011

Ans. (b) :

16. Maximum number of edges in a n-node undirected graph without self-loops is

(a) n^2 (b) $n(n-1)/2$
(c) $n(n-1)$ (d) $n(n+1)/2$

RPSC Lect. 2011

Ans. (b) :

17. Level order traversal of a rooted tree can be done by starting from the root and performing

(a) preorder traversal (b) in-order traversal
(c) depth first search (d) breadth first search

RPSC Lect. 2011

Ans. (d) :

18. Which of the following is not a backtracking algorithm?

(a) Knight tour problem
(b) N-queen problem
(c) Towers of Hanoi
(d) M-coloring problem

UPPSC LT GRADE 29.07.2018

Ans. (c) :

19. Which of the following is useful in traversing a given graph by breadth-first search (BFS)?

(a) Stack (b) Set
(c) List (d) Queue

UPPSC LT GRADE 29.07.2018

Ans. (d) :

20. Which of the following is not a primitive data type?

(a) Boolean (b) Byte
(c) String (d) Double

UPPSC LT GRADE 29.07.2018

Ans. (c) :

21. While implementing a stack on a register stack, the stack pointer register is

(a) incremented first during push operation
(b) decremented first during push operation
(c) incremented first during pop operation
(d) decremented first during pop operation

UPPSC LT GRADE 29.07.2018

Ans. (a) :

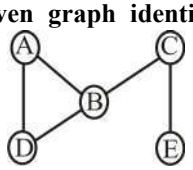
22. Zero address instructions are implemented with the help of

(a) queue (b) stack
(c) register (d) None of the above

UPPSC LT GRADE 29.07.2018

Ans. (b) :

23. In the given graph identify the cut vertices:



(a) B and E (b) C and D
(c) A and E (d) C and B

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Ans. (d) :

24. From a complete graph by removing maximum _____ edges, we can construct a spanning tree.

(a) e – n + 1 (b) n – e + 1
(c) n + e –1 (d) e –n –1

UPPSC LT GRADE 29.07.2018

Ans. (a) :

25. Which one of the following is prefix representation of the infix expression A*(B+C)/D?

(a) /*A+BCD (b) A + B/CD
(c) + *AB/CD (d) None of the above

UPPSC LT GRADE 29.07.2018

Ans. (d) :

26. A B-tree is of order p and consists of n keys. Its maximum height is

(a) $\log_{(p/2)}{}^{(n+1)}/2$ (b) $\log p^n$
(c) $\log(p/2)^{(n+1)}$ (d) None of the above

UPPSC LT GRADE 29.07.2018

Ans. (b) :

27. The following postfix expression with single-digit operands is evaluated using a stack:

823^/23*+51*–

(Note that ^ is the exponentiation operator.) The top two elements of the stack after the first * is evaluated, are

(a) 6, 1 (b) 5,7
(c) 3,2 (d) 1,5

UPPSC LT GRADE 29.07.2018

Ans. (a) :

28. A hash function defined as f(key)=key mod 7 with linear probing is used to insert the keys 37, 38, 72, 48, 98, 11, 56 into a table indexed from 0 to 6. What will be the location of key 11?

(a) 3 (b) 4
(c) 5 (d) 6

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Ans. (c) :

29. The concatenation of two lists is to be performed in O(1) time. Which of the following implementations of lists could be used?

(a) Singly linked list
(b) Doubly linked list
(c) Circular doubly linked list
(d) Array implementation of list

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Ans. (c) :

30. Match List-I with List-II and select the correct answer using the codes given below the Lists:

List-I		List-II	
A.	All-pairs shortest path	1.	Greedy
B.	Quicksort	2.	Depth-first search
C.	Minimum weight spanning tree	3.	Dynamic programming
D.	Connected components	4.	Divide and conquer

Codes

(a) A B C D
2 4 1 3
(b) A B C D
3 4 1 2
(c) A B C D
3 4 2 1
(d) A B C D
4 1 2 3

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Ans. (b) :

31. What is common in three different types of traversals (inorder, preorder and postorder)?

(a) Root is visited before right subtree
(b) Left subtree is always visited before right subtree
(c) Root is visited after left subtree
(d) All of the above

UPPSC LT GRADE 29.07.2018

Ans. (b) :

32. Which of the following is correct recurrence relation for worst case of binary search?

(a) T(n)=2T(n/2)+O(1)
T(1)=T(O)=O(1)
(b) T(n)=T(n/2)+O(n)
T(1)=T(O)=O(1)
(c) T(n)=T(n/2)+O(1)
T(1)=T(O)=O(1)
(d) T(n)=T(n/2)+O(logn)
T(1)=T(O)=O(1)

UPPSC LT GRADE 29.07.2018

Ans. (c) :

33. Which of the following traversal techniques lists the nodes of a binary search tree in ascending order?

(a) Postorde (b) Preorder
(c) Inorder (d) None of the above

UPPSC LT GRADE 29.07.2018

Ans. (c) :

34. A hash table of length 10 uses open addressing with hash function h(k)=kmod10 and linear probing. After inserting 6 values into an empty hash table, the table is shown below:

0	
1	
2	42
3	23
4	34
5	52
6	46
7	33
8	
9	

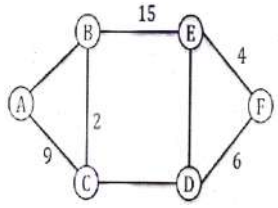
Which of the following choices gives a possible order in which the key values could have been inserted in the table?

(a) 46, 42, 34, 52, 23, 33
(b) 34, 42, 23, 52, 33, 46
(c) 46, 34, 42, 23, 52, 33
(d) 42, 46, 33, 23, 34, 52

UPPSC LT GRADE 29.07.2018

Ans. (c) :

35. The graph shown below has 8 edges with distinct integer edge weights. The minimum spanning tree (MST) is of weight 36 and contains the edges: { (A C), (B, C), (B, E), (E, F), (D, F)}. The edge weights of only those edges which are in the MST are given in the figure shown below. The minimum possible sum of weights of all 8 edges of this graph is.....



GATE 2015 (Shift-I)

Ans. 69

36. The recurrence relation for the optimal execution time of the Tower of Hanoi problem having n discs is

(a) $T(n) = 2\,T(n-2) + 2$

(b) $T(n) = 2T(n-1) + n$

(c) $T(n) = 2T\left(\frac{n}{3}\right) + 1$

(d) $T(n) = 2T(n-1) + 1$

UPSC Senior Scientific Officer Grade-II 16.07.2017

Ans. (d) :

37. The recurrence relation capturing the optimal execution time of the Towers of Hanoi problem with n discs is

(a) $T(n) = 2T(n-2) + 2$ (b) $T(n) = 2T(n-1) + n$

(c) $T(n) = 2T(n/2) + 1$ (d) $T(n) = 2T(n-1) + 1$

APPSC Lect. Degree College 07.06.2017 (CS)

Ans. (d) :

38. Two labeled trees are isomorphic if _____

(a) graphs of the two trees are isomorphic

(b) the two trees have same label

(c) Both (a) and (b)

(d) graphs of the two trees are cyclic

GPSC Asstt. Prof. 30.06.2016

Ans. (c) :

39. A circular list can be used to represent

(a) Graph (b) Stack

(c) Queue (d) Tree

UPPCL AE 2014

Ans. (b) :

40. The prefix form of A+B/ (C * D ^ E) is

(a) +ABCD*^DE (b) +A/B*C^DE

(c) +/*^ACBDE (d) +A/BC*^DE

UPPCL AE 2014

Ans. (b) :

41. Choose the equivalent prefix form of the following expression $(a + (b\text{-}c))^* ((d\text{-}e)/(f + g - h))$

(a) *+a-bc/-de- +fgh

(b) *+a-bc-/de-+fgh

(c) *+a-bc/-ed+-fgh

(d) *+ab-c/-ed+-fgh

ISRO Scientist/Engineer 2017 (May)

Ans. (a) :

42. The infix expression A + (B–C)* D is correctly represented in prefix notations as

(a) A+ B– C* D (b) +A* –BCD

(c) ABC–D* + (d) A+BC–D*

ISRO Scientist/Engineer 2009

Ans. (c) :

43. Given an undirected graph G with V vertices and E edges, the sum of the degrees of all vertices is

(a) E (b) 2E

(c) V (d) 2V

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (b) :

44. Which of the following is an advantage of adjacency list representation over adjacency matrix representation of a graph?

(a) In adjacency list representation, space is saved for sparse graphs.

(b) Deleting a vertex in adjacency list representation is easier than adjacency matrix representation.

(c) Adding a vertex in adjacency list representation is easier than adjacency matrix representation.

(d) All of the option

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (d) :

45. A path in graph G, which contains every vertex of G once and only once?

(a) Eular Circuit (b) Hamiltonian Path

(c) Eular Path (d) Hamiltonian Circuit

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (b) :

46. What are the appropriate data structures for graph traversal using Breadth First Search (BFS) and Depth First Search (DFS) algorithms?

(a) Stack for BFS and Queue for DFS

(b) Queue for BFS and Stack for DFS

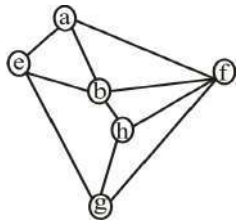
(c) Stack for BFS and Stack for DFS

(d) Queue for BFS and Queue for DFS

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (b) :

47. In a given following graph among the following sequences:



(I) a b e g h f

(II) a b f e h g

(III) a b f h g e

(IV) a f g h b e

Which are depth first traversals of the above graph?

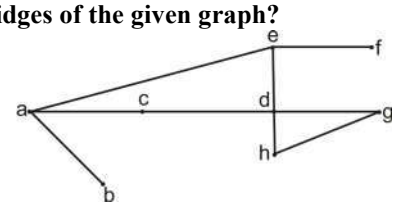
(a) I, II and IV only (b) I and IV only

(c) II, III and IV only (d) I, III and IV only

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (d) :

48. Considering the following graph, which one of the following set of edges represents all the bridges of the given graph?



(a) (a,b), (e,f) (b) (a,b), (a,c)

(c) (c,d), (d,h) (d) (a,b)

NIELIT Scientists-B 22.07.2017 (IT)

Ans. (a) :

49. In the _____ traversal we process all of a vertex's descendants before we move to and adjacent vertex.

(a) Depth First (b) Breadth First
(c) Width First (d) Depth Limited

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (a) :

50. What data structure is used for depth first traversal of a graph?

(a) Queue (b) Stack
(c) List (d) None of above

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (b) :

51. A _____ is a linear list in which insertions and deletions are made to from either end of the structure

(a) Circular queue (b) Priority queue
(c) Stack (d) Dequeue

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (d) :

52. The recurrence relation capturing the optimal execution time of the Towers of Hanoi problem with n discs is:

(a) T(n)=2T(n–2)+2 (b) T(n)=2T(n/2)+1
(c) T(n)=2T(n–2)+n (d) T(n)=2T(n–1)+1

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (d) :

53. Which of the following is the correct order of evaluation for the below expression?

z = x+y*z/4%2–1

(a) * / % + – = (b) = * / % + –
(c) / * % – + = (d) * % / – + =

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (a) :

54. The number of unused pointers in a complete binary tree of depth 5 is:

(a) 4 (b) 8
(c) 16 (d) 32

NIELIT Scientists-B 04.12.2016 (CS)

Ans. (c) :

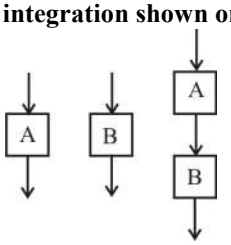
55. In a complete k-ary tree, every internal node has exactly k children. The number of leaves in such a tree with n internal nodes is

(a) nk (b) (n-1) k + 1
(c) n (k - 1) + 1 (d) n (k - 1)

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

56. The Cyclomatic complexity of each of the modules A and B shown below is 10. What is the Cyclomatic complexity of the sequential integration shown on the right hand side ?



(a) 19 (b) 21
(c) 20 (d) 10

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (a) :

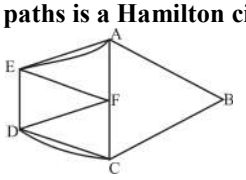
57. Let G be a graph with n vertices and m edges. What is the tightest upper bound on the running time on Depth First Search of G? Assume that the graph is represented using adjacency matrix.

(a) O (n) (b) O (m + n)
(c) $O(n^2)$ (d) O(mn)

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

58. For the graph shown, which of the following paths is a Hamilton circuit?



(a) ABCDCFDEFAEA (b) AEDCBAF
(c) AEFDCBA (d) AFCDEBA

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

59. If G is an undirected planar graph on n vertices with e edges then

(a) e<=n (b) e<=2n
(c) e<=3n (d) None of the option

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

60. Choose the most appropriate definition of plane graph.

(a) A simple graph which is isomorphic to Hamiltonian graph
(b) A graph drawn in a plane in such a way that if the vertex set of graph can be partitioned into two non-empty disjoint subset X and Y in such a way that each edge of G has one end In X and one end in Y
(c) A graph drawn in plane in such a way that any pair of edges meet only at their end vertices
(d) None of the option

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

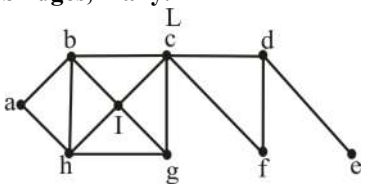
61. A Queue is implemented using an array such that ENQUEUE and DEQUEUE operations are performed efficiently. Which one of the following statement is CORRECT (n refers to the number of times in the queue)?

(a) Both operations can be performed in O (1) time
(b) At most one operation can be performed in O (1) time but the worst case time for the other operation will be Ω (n)
(c) The worst case time complexity for both operations will be Ω (n)
(d) Worst case time complexity for both operations will be Ω (logn)

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (a) :

62. Consider the following graph L and find the bridges, if any.



(a) No bridge (b) {d, e}
(c) {c, d} (d) {c ,d} and {c, f}

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (b) :

63. A balance factor in AVL tree is used to check
(a) What rotation to make.
(b) if all child nodes are at same level.
(c) when the last rotation occurred.
(d) if the tree is unbalanced.

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (a) :

64. A priority queue is implemented as a Max-Heap. Initially, it has 5 elements. The level-order traversal of the heap is : 10, 8, 5, 3, 2. Two new elements 1 and 7 are inserted into the heap in that order. The level-order traversal of the heap after the insertion of the elements is
(a) 10, 8, 7, 3, 2, 1, 5 (b) 10, 8, 7, 2, 3, 1, 5
(c) 10, 8, 7, 1, 2, 3, 5 (d) 10, 8, 7, 5, 3, 2, 1

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (a) :

65. Which of the following statements is/are TRUE for an undirected graph?
P : Number of odd degree vertices is even
Q: Sum of degrees of all vertices is even
(a) P only (b) Q only
(c) Both P and Q (d) Neither P nor Q

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

66. Consider the following function that takes reference to head of a Doubly Linked List as parameter. Assume that a node of doubly linked list has previous pointer as prev and next pointer as next.

```
Void fun (struct node **head__ ref)
{
  struct node *temp = NULL;
  struct node *current = *head_ref;
    while (current ! = NULL)
{
  temp = current->prev;
  current->prev = current->next;
  current->next = temp;
  current = current-> prev;
}
  if(temp !=NULL)
    *head_ref = temp->prev;
}
```

Assume that reference of head of following doubly linked list is passed to above function
1<--> 2 <--> 3 <--> 4 <--> 5 <--> 6. What should be the modified linked list after the function call?
(a) 2 <--> 1 <--> 4 <--> 3 <--> 6 <--> 5
(b) 5 <--> 4 <--> 3 <--> 2 <--> 1 <--> 6
(c) 6 <--> 5 <--> 4 <--> 3 <--> 2 <--> 1
(d) 6 <--> 5 <--> 4 <--> 3 <--> 1 <--> 2

NIELIT Scientists-B 22.07.2017 (CS)

Ans. (c) :

67. The maximum number of nodes in a binary tree of level k, k ≥ 1 is:
(a) 2^k+1 (b) 2^{k-1}
(c) 2^k-1 (d) $2^{k-1}-1$

NIELIT Scientists-B 04.12.2016 (IT)

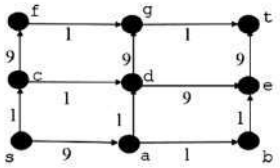
Ans. (c) :

68. Let G be a simple undirected planar graph on 10 vertices with 15 edges. If G is a connected graph, then the number of bounded faces in any embedding of G on the plane is equal to :
(a) 3 (b) 4
(c) 5 (d) 6

NIELIT Scientists-B 04.12.2016 (IT)

Ans. (d) :

69. In a directed acyclic graph with a source vertex s, the quality-score of a directed path is defined to be the product of the weights of the edges on the path. Further, for a vertex v other than s, the quality-score of v is defined to be the maximum among the quality-scores of all the paths from s to v. The quality-score of s is assumed to be 1.

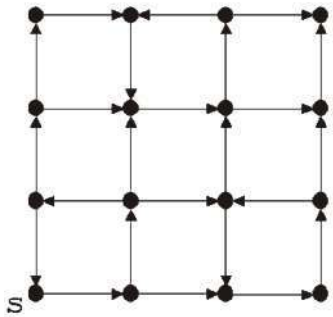


The sum of the quality-scores of al the vertices in the graph shown above is _____.

GATE 2021 (Shift-II)

Ans. 929 to 929

70. Consider the following directed graph:



Which of the following is/are correct about the graph?
(a) The graph does not have a topological order.
(b) A depth-first traversal starting at vertex S classifies three directed edges as back edges.

(c) The graph does not have a strongly connected component.
(d) For each pair of vertices u and v, there is a directed path from u to v.

GATE 2021 (Shift-II)

Ans. (a; b) :

71. For constants a ≥ 1 and b > 1, consider the following recurrence defined on the non-negative integers:

$$T(n) = a \cdot T\left(\frac{n}{b}\right) + f(n)$$

Which one of the following options is correct about the recurrence T(n)?

(a) If $f(n)$ is $n \log_2(n)$, then T(n) is $\Theta(n \log_2(n))$.

(b) If $f(n)$ is $\frac{n}{\log_2(n)}$, then T(n) is $\Theta(\log_2(n))$.

(c) If $f(n)$ $O\left(n^{\log_b(a)-\epsilon}\right)$ for some $\epsilon > 0$, then T(n) is $\Theta\left(n^{\log_b(a)}\right)$.

(d) If $f(n)$ is $\Theta\left(n^{\log_b(a)}\right)$, then T(n) is $\Theta\left(n^{\log_b(a)}\right)$.

GATE 2021 (Shift-II)

Ans. (c) :

72. Consider a complete binary tree with 7 nodes. Let A denote the set of first 3 elements obtained by performing Breadth-First Search (BFS) starting from the root. Let B denote the set of first 3 elements obtained by performing Depth-First Search (DFS) starting from the root.
The value of |A – B| is)_____.

GATE 2021 (Shift-II)

Ans. 1 to 1

73. What is the worst-case number of arithmetic operations performed by recursive binary search on a sorted array of size n?

(a) $\Theta\left(\sqrt{n}\right)$ (b) $\Theta(\log_2(n))$

(c) $\Theta(n^2)$ (d) $\Theta(n)$

GATE 2021 (Shift-II)

Ans. (c) :

74. Let G be a connected undirected weighted graph. Consider the following two statements.
S_1 : There exists a minimum weight edge in G which is present in every minimum spanning tree of G.
S_2 : If every edge in G has distinct weight, then G has a unique minimum spanning tree.
Which one of the following options is correct?

(a) Both S_1 and S_2 are true.
(b) S_1 is true and S_2 is false.
(c) S_1 is false and S_2 is true.
(d) Both S_1 and S_2 are false.

GATE 2021 (Shift-II)

Ans. (a) :

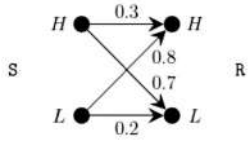
75. Let H be a binary min-heap consisting of n elements implemented as an array. What is the worst case time complexity of an optimal algorithm to find the maximum element in H?

(a) $\Theta(1)$ (b) $\Theta(\log n)$
(c) $\Theta(n)$ (d) $\Theta(n \log n)$

GATE 2021 (Shift-II)

Ans. (b) :

76. A sender (S) transmits a signal, which can be one of the two kinds: H and L with probabilities 0.1 and 0.9 respectively, to a receiver (R).
In the graph below, the weight of edge (u, v) is the probability of receiving v when u is transmitted, where u, v ∈ {H, L}. For example, the probability that are received signal is L given the transmitted signal was H, is 0.7.



If the received signal is H, the probability that the transmitted signal was H (rounded to 2 decimal places) is _____.

GATE 2021 (Shift-I)

Ans. 0.04 to 0.04

77. Define R_n to be the maximum amount earned by cutting a rod of length n meters into one or more pieces of integer length and selling them. For i > 0, let p[i] denote the selling price of a rod whose length is i meters. Consider the array of prices:
p[1] = 1, p[2] = 5, p[3] = 8, p[4] = 9, p[5] = 10, p[6] = 17, p[7] = 18
Which of the following statements is/are correct about R_7?

(a) $R_7 = 18$
(b) $R_7 = 19$
(c) R_7 is achieved by three different solutions.
(d) R_7 cannot be achieved by a solution consisting of three pieces.

GATE 2021 (Shift-I)

Ans. (a, c) :

78. An articulation point in a connected graph is a vertex such that removing the vertex and its incident edges disconnects the graph into two or more connected components.
Let T be a DFS tree obtained by doing DFS in a connected undirected graph G.
Which of the following options is/are correct?

(a) Root of T can never be an articulation point in G.
(b) Root of T is an articulation point in G if and only if it has 2 or more children.
(c) A leaf of T can be an articulation point in G.
(d) If u is an articulation point in G such that x is an ancestor of u in T and y is a descendent of u in T, then all paths from x to y in G must pass through u.

GATE 2021 (Shift-I)

Ans. (b) :

79. Let G = (V, E) be an undirected unweighted connected graph. The diameter of G is defined as:

$diam(G) = \max_{u,v \in V} \{$the length of shortest path between u and v$\}$

Let M be the adjacency matrix of G.

Define graph G_2 on the same set of vertices with adjacency matrix N, where

$$N_{ij} = \begin{cases} 1 & \text{if } M_{ij} > 0 \text{ or } P_{ij} > 0, \text{ where } P = M^2 \\ 0 & \text{otherwise} \end{cases}$$

Which one of the following statements is true?

(a) $diam(G_2) \le \lceil diam(G)/2 \rceil$
(b) $\lceil diam(G)/2 \rceil < diam(G_2) < diam(G)$
(c) $diam(G_2) = diam(G)$
(d) $diam(G) < diam(G_2) \le 2\, diam(G)$

GATE 2021 (Shift-I)

Ans. (a) :

80. Consider the following sequence of operations on an empty stack.

push(54); push(52); pop(); push(55). push(62); s = pop();

Consider the following sequence of operations on an empty queue.

enqueue(21); enqueue(24); dequeue(); enqueue(28); enqueue(32); q = dequeue();

The value of s + q is _____.

GATE 2021 (Shift-I)

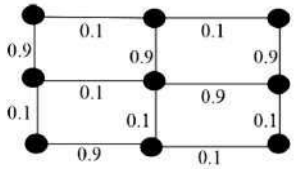
Ans. 86 to 86

81. In an undirected connected planar graph G, there are eight vertices and five faces. The number of edges in G is _____.

GATE 2021 (Shift-I)

Ans. 11 to 11

82. Consider the following undirected graph with edge weights as shown:



The number of minimum-weight spanning trees of the graph is _____

GATE 2021 (Shift-I)

Ans. 3 to 3

83. A binary search tree T contains n distinct elements. What is the time complexity of picking an element in T that is smaller than the maximum element in T?

(a) $\Theta(n \log n)$ (b) $\Theta(n)$
(c) $\Theta(\log n)$ (d) $\Theta(1)$

GATE 2021 (Shift-I)

Ans. (d) :

84. Let P be an array containing n integers. Let t be the lowest upper bound on the number of comparisons of the array elements, required to find the minimum and maximum values in an arbitrary array of n elements. Which one of the following choices is correct?

(a) $t > 2n - 2$
(b) $t > 3\left\lceil \frac{n}{2} \right\rceil$ and $t \le 2n - 2$
(c) $t > n$ and $t \le 3\left\lceil \frac{n}{2} \right\rceil$
(d) $t > \lceil \log_2(n) \rceil$ and $t \le n$

GATE 2021 (Shift-I)

Ans. (c) :

85. Consider the following three functions.

$f_1 = 10^n \quad f_2 = n^{\log n} \quad f_3 = n^{\sqrt{n}}$

Which one of the following options arranges the functions in the increasing order of asymptotic growth rate?

(a) f_3, f_2, f_1 (b) f_2, f_1, f_3
(c) f_1, f_2, f_3 (d) f_2, f_3, f_1

GATE 2021 (Shift-I)

Ans. (d) :

86. Graph G is obtained by adding vertex s to $K_{3,4}$ and making s adjacent to every vertex of $K_{3,4}$. The minimum number of colours required to edge-colour G is _____.

GATE 2020

Ans. 7 to7

87. Consider a graph G = (V, E), where $V = \{v_1, v_2, ..., v_{100}\}$, $E = \{(v_i, v_j) \mid 1 \le i < j \le 100\}$, and weight of the age (v_i, v_j) is $|i - j|$. The weight of minimum spanning tree of G is _____.

GATE 2020

Ans. 99 to 99

88. Consider the array representation of a binary min-heap containing 1023 elements. The minimum number of comparisons required to find the maximum in the heap is _____.

GATE 2020

Ans. 511 to 511

89. Let G = (V, E) be a directed, weighted graph with weight function $w: E \to \mathbb{R}$. For some function $f: V \to \mathbb{R}$, for each edge $(u,v) \in E$, define $w'(u, v)$ as $w(u, v) + f(u) - f(v)$.

Which one of the options completes the following sentence so that it is TRUE?

"The shortest path in G under w are shortest paths under w' too, _____".

(a) for every $f: V \to \mathbb{R}$
(b) if and only if $\forall u \in V$, $f(u)$ is positive
(c) if and only if $\forall u \in V$, $f(u)$ is negative
(d) if and only if $f(u)$ is the distance from s to u in the graph obtained by adding a new vertex s to G and edges of zero weitht from s to every vertex of G

GATE 2020

Ans. (a) :

90. In a balanced binary search tree with n elements, what is the worst case time complexity of reporting all elements in range [a, b]? Assume that the number of reported elements is k.

(a) $\Theta(\log n)$ (b) $\Theta(\log n + k)$
(c) $\Theta(k \log n)$ (d) $\Theta(n \log k)$

GATE 2020

Ans. (b) :

91. Let G = (V, E) be a weighted undirected graph and let T be a Minimum Spanning Tree (MST) of G maintained using adjacency lists. Suppose a new weighted edge (u, v) ∈ V × V is added to G. The worst case time complexity of determining if T is still an MST of the resultant graph is

(a) $\Theta(|E| + |V|)$ (b) $\Theta(|E||V|)$
(c) $\Theta(E| \log|V|)$ (d) $\Theta(|V|)$

GATE 2020

Ans. (d) :

92. Consider a double hashing scheme in which the primary hash function is $h_1(k) = k \bmod 23$, and the secondary hash function is $h_2(k) = 1 + (k \bmod 19)$. Assume that the table size is 23. Then the address returned by probe 1 in the probe sequence (assume that the probe sequence begins at probe 0) for key value k = 90 is ____.

GATE 2020

Ans. 13 to 13

93. What is the worst case time complexity of inserting n elements into an empty linked list, if the linked list needs to be maintained in sorted order?

(a) $\Theta(n)$ (b) $\Theta(n \log n)$
(c) $\Theta(n^2)$ (d) $\Theta(1)$

GATE 2020

Ans. (c) :

94. The preorder traversal of a binary search tree is 15, 10, 12, 11, 20, 18, 16, 19. Which one of the following is the postorder traversal of the tree?

(a) 10, 11, 12, 15, 16, 18, 19, 20
(b) 11, 12, 10, 16, 19, 18, 20, 15
(c) 20, 19, 18, 16, 15, 12, 11, 10
(d) 19, 16, 18, 20, 11, 12, 10, 15

GATE 2020

Ans. (b) :

95. The pre-order traversal of a binary search tree is given by 12,8,6,2,7,9,10,16,15,19,17,20. Then the post-order traversal of this tree is:

(a) 2,6,7,8,9,10,12,15,16,17,19,20
(b) 2,7,6,10,9,8,15,17,20,19,16,12
(c) 7,2,6,8,9,10,20,17,19,15,16,12
(d) 7,6,2,10,9,8,15,16,17,20,19,12

GATE 2017 (Shift-II)

Ans. (b) :

96. Consider the recurrence function

$$T(n) \begin{cases} 2T(\sqrt{n}+1, & n > 2 \\ 2, & 0 < n \le 2 \end{cases}$$

Then T (n) in terms of Θ notation is

(a) $\Theta(\log \log n)$ (b) $\Theta(\log n)$
(c) $\Theta(\sqrt{n})$ (d) $\Theta(n)$

GATE 2017 (Shift-II)

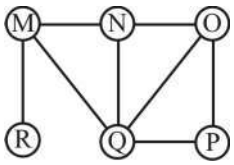
Ans. (b) :

97. G is an undirected graph with n vertices and 25 edges such that each vertex of G has degree at least 3. Then the maximum possible value of n is _____.

GATE 2017 (Shift-II)

Ans. 16.0 to 16.0

98. The Breadth First Search (BFS) algorithm has been implemented using the queue data structure. Which one of the following is a possible order of visiting the nodes in the graph below?



(a) MNOPQR (b) NQMPOR
(c) QMNROP (d) POQNMR

GATE 2017 (Shift-II)

Ans. (d) :

99. Given the following binary number in 32-bit (single precision) IEEE-754 format:
00111110011011010000000000000000
The decimal value closest to this floating-point number is

(a) 1.45×10^{1} (b) 1.45×10^{-1}
(c) 2.27×10^{-1} (d) 2.27×10^{1}

GATE 2017 (Shift-II)

Ans. (c) :

100. A circular queue has been implemented using a singly linked list where each node consists of a value and a single pointer pointing to the next node. We maintain exactly two external pointers FRONT and REAR pointing to the front node and the rear node of the queue, respectively. Which of the following statements is/are CORRECT for such a circular queue, so that insertion and deletion operations can be performed in 0 (1) time?

I. Next pointer of front node points to the rear node.
II. Next pointer of rear node points to the front node

(a) I only (b) II only
(c) Both I and II (d) Neither I nor II

GATE 2017 (Shift-II)

Ans. (b) :

101. Suppose c = <c[0]…….,c[k - 1]> is an array of length k, where all the entries are from the set {0,1}. For any positive integers a and n, consider the following pseudocode.

```
DOSOMETHING (c,a,n)
z←1
for i ← 0 to k – 1
    do z←z^2 mod n
      if c[i] = 1
           then z←(z×a) mod n
return z
```

If k = 4, c = <1,0,1,1>, a = 2 and n = 8, then the output of DOSOMETHING (c,a,n) is

GATE 2015 (Shift-III)

Ans. 0

102. Consider a B+ tree in which the search key is 12 bytes long, block size is 1024 bytes, record pointer is 10 bytes long and block pointer 8 bytes longs. The maximum number of keys that can be accommodated in each non-leaf node of the tree is_____

GATE 2015 (Shift-III)

Ans. 50

103. Let G be a connected undirected graph of 100 vertices and 300 edges. The weight of a minimum spanning tree of G is 500. When the weight of each edge of G is increased by five, the weight of a minimum spanning tree becomes_____.

GATE 2015 (Shift-III)

Ans. 995

104. Assume that a mergesort algorithm in the worst case takes 30 seconds for an input of size 64. Which of the following most closely approximates the maximum input size of a problem that can be solved in 6 minutes?

(a) 256 (b) 512
(c) 1024 (d) 2048

GATE 2015 (Shift-III)

Ans. (b) :

105. Consider a binary tree T that has 200 leaf nodes. Then, the number of nodes in T that have exactly two children are _____.

GATE 2015 (Shift-III)

Ans. 199

106. Consider a software project with the following information domain characteristics for calculation of function point metric.

Number of external inputs (I) = 30
Number of external outputs (O) = 60
Number of external inquiries (E) = 23
Number of files (F) = 08
Number of external interfaces (N) = 02

It is given that the complexity weighting factors for I, O, E, F and N are 4, 5, 4, 10 and 7, respectively. It is also given that, out of fourteen value adjustment factors that influence the development effort, four factors are not applicable, each of the other four factors have value 3, and each of the remaining factors have value 4. The computed value of function point metric is _____.

GATE 2015 (Shift-III)

Ans. 612 to 613

107. Consider the following array of elements.
(89, 19, 50, 17, 12, 15, 2, 5, 7, 11, 6, 9, 100)
The minimum number of interchanges needed to convert it into a max-heap is

(a) 4 (b) 5
(c) 2 (d) 3

GATE 2015 (Shift-III)

Ans. (d) :

108. The result evaluating the postfix expression 10 5 + 60 6 / * 8 – is

(a) 284 (b) 213
(c) 142 (d) 71

GATE 2015 (Shift-III)

Ans. (c) :

109. While inserting the elements 71, 65, 84, 69, 69, 83 in an empty binary search tree (BST) in the sequenceshown, the elements in the lowest level is-

(a) 65 (b) 67
(c) 69 (d) 83

GATE 2015 (Shift-III)

Ans. (b) :

110. Let G be a connected planar graph with 10 vertices. If the number of edges on each face is three, then the number of edges in G is_____

GATE 2015 (Shift-I)

Ans. 24

111. The least number of temporary variables required to create a three address code in static single assignment from for the expression q+r/3+s-t*5+u*v/w is___

GATE 2015 (Shift-I)

Ans. 2

112. Let G = (V, E) be a simple undirected graph and s be a particular vertex in it called the source. For x ∈ V, let d(x) denote the shortest distance in G from s to x. A breadth first search (BFS) is performed starting at s. Let T be the resultant BFS tree. If (u, v) is an edge of G that is not in T, then which one of the following CANNOT be the value of d(u)-d(v)?

(a) -1 (b) 0
(c) 1 (d) 2

GATE 2015 (Shift-I)

Ans. (d) :

113. Consider a max heap, represented by the array: 40, 30, 20, 10, 15, 16, 17, 8, 4

Array Index	1	2	3	4	5	6	7	8	9
Value	40	30	20	10	15	16	17	8	4

Now consider that a value 35 is inserted into this heap. After insertion, the new heap is

(a) 40, 30, 20, 10, 15, 16, 17, 8, 4, 35
(b) 40, 35, 20, 10, 30, 16, 17, 8, 4, 15
(c) 40, 30, 20, 10, 35, 16, 17, 8, 4, 15
(d) 40, 35, 20, 10, 15, 16, 17, 8, 4, 30

GATE 2015 (Shift-I)

Ans. (b) :

114. The height of a tree is the length of the longest root-to-leaf path in it. The maximum and minimum number of nodes in a binary tree of height 5 are

(a) 63 and 6 respectively
(b) 64 and 5, respectively
(c) 32 and 6, respectively
(d) 31 and 5, respectively

GATE 2015 (Shift-I)

Ans. (a) :